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Paper 10
Date: October 3, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NOKIA OF AMERICA CORPORATION
Petitioner,

v.

TQ DELTA, LLC,
Patent Owner.

IPR2022-00665
Patent 7,836,381 B1

Before JONI Y. CHANG, LYNNE E. PETTIGREW, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Nokia of America Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–8 ("the challenged claims") of U.S. Patent No. 7,836,381 B1 (Ex. 1001, "the '381 patent"). TQ Delta, LLC ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition. With our authorization, Petitioner filed a Reply (Paper 8, "Reply") to the Preliminary Response, and Patent Owner filed a Sur-reply (Paper 9, "Sur-reply") to the Reply.

An *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Further, a decision to institute may not institute on fewer than all claims challenged in the petition. 37 C.F.R. § 42.108(a). Based on the arguments and evidence of record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one of the challenged claims of the '381 patent is unpatentable. Accordingly, we institute an *inter partes* review as to the challenged claims of the '381 patent on all the grounds of unpatentability in the Petition.

B. Real Parties in Interest

Petitioner identifies the following real parties in interest: 1) Nokia Corporation; 2) Nokia Solutions and Networks Oy; and 3) Nokia of America Corporation. Pet. 80. Patent Owner identifies itself as the only real party in interest. Paper 5, 2.

C. Related Matters

The parties indicate that the '381 patent is the subject of the following district court cases: 1) *TQ Delta, LLC v. 2Wire, Inc.*, No. 1:13-cv-01835 (D. Del.); 2) *TQ Delta, LLC v. ADTRAN, Inc.*, No. 1:14-cv-00954 (D. Del.); and 3) *ADTRAN, Inc. v. TQ Delta, LLC*, No. 1:15-cv-00121 (D. Del.). Pet. 80; Paper 5, 2–3.

D. The '381 Patent

The '381 patent relates to "memory sharing in communication systems." Ex. 1001, 1:19–21. The '381 patent describes a system designed to allocate a first portion of a shared memory to an interleaver and a second portion of the shared memory to a deinterleaver. *Id.* at 5:33–39. The system may determine a maximum amount of shared memory that can be allocated to an interleaver or a deinterleaver. *Id.* at 2:3–6. The system may determine an amount of memory required to interleave or deinterleave a first plurality of Reed-Solomon (RS) coded data bytes and an amount of memory required to interleave or deinterleave a second plurality of RS coded data bytes and allocate the shared memory accordingly. *See id.* at 6:20–7:3.

E. Illustrative Claim

Of the challenged claims, claims 1 and 5 are independent. Claim 1 is reproduced below.

> 1. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:
>
> transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

> determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
>
> allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;
>
> allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and
>
> interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

Ex. 1001, 10:43–11:4.

F. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
Declaration of Richard Wesel ("Wesel Declaration")	1003
Mazzoni, US 7,269,208 B2, issued Sept. 11, 2007 ("Mazzoni")	1005
Fadavi-Ardekani, US 6,707,822 B1, issued Mar. 16, 2004 ("Fadavi-Ardekani")	1006
European Telecommunications Standards Institute, ETSI TS 101 270-2 V1.2.1 (2003) ("VDSL1")	1007

G. Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–8	103	Mazzoni, VDSL1
1–8	103	VDSL1, Fadavi-Ardekani

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art would have had

> at least a Bachelor's degree in electrical engineering, or a related field, and at least 6–7 years of experience in telecommunications or related field; a master's degree in electrical or computer engineering, or the equivalent, and at least 3–4 years of experience in telecommunications or related field; or a Ph.D. in electrical or computer engineering, or the equivalent, with at least 1–2 years of experience in telecommunications or related field.

Pet. 10 (citing Ex. 1003 ¶ 16). Petitioner's description of the level of ordinary skill in the art is supported by the testimony of Petitioner's declarant, Dr. Richard Wesel. Ex. 1003 ¶ 16. Patent Owner does not propose a description of the level of ordinary skill in the art or dispute Petitioner's description. We adopt Petitioner's description for purposes of this Decision.

B. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same standard used in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of the claim as understood by one of ordinary skill in the art and the

prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). The parties propose constructions for several claim terms and phrases. Pet. 6–9; Prelim. Resp. 38–42; Reply 9–10; Sur-reply 8–10. We determine that no claim terms or phrases require express construction to resolve the parties' disputes about the asserted grounds of unpatentability at this stage of the proceeding. *See* Sections II.E, II.F.

C. 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 314(a) to deny the Petition based on a parallel district court proceeding. Prelim. Resp. 28–38; Sur-reply 7–8. Section 314(a) states that

> [t]he Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Under § 314(a), we have discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016).

We consider several factors when determining whether to deny institution under § 314(a) based on a parallel district court proceeding. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"). Nonetheless, "where the PTAB determines that the information presented at the institution stage presents a compelling unpatentability challenge, that determination alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*." USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, 4–5 (June 21, 2022), *available at* https://www.uspto.gov/sites/default/files/documents/

interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf. "Compelling, meritorious challenges are those in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence." *Id.* at 4.

Based on the evidence of record, Petitioner's assertion that claims 1–8 would have been obvious over Mazzoni and VDSL1 presents a compelling unpatentability challenge. At this stage of the proceeding, Patent Owner disputes that the Mazzoni and VDSL1 combination teaches a "shared memory" and "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to" an interleaver or deinterleaver. Prelim. Resp. 42–44, 50–53. Patent Owner also disputes that it would have been obvious to combine the cited teachings of Mazzoni and VDSL1. *Id.* at 54–58. As discussed in detail below, the evidence of record plainly shows that the Mazzoni and VDSL1 combination teaches the disputed limitations and that it would have been obvious to combine the cited teachings of Mazzoni and VDSL1. *See* Sections II.E.1, II.E.3. Because the information presented at the institution stage presents a compelling unpatentability challenge, we decline to exercise our discretion under § 314(a) to deny the Petition.

D. 35 U.S.C. § 315(b)

Patent Owner argues that we should deny the Petition under 35 U.S.C. § 315(b). Prelim. Resp. 23. Section 315(b) provides that an *inter partes* review "may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging

infringement of the patent." Patent Owner served 2Wire, Inc. ("2Wire") with a complaint alleging infringement of the '381 patent in February 2014. Prelim. Resp. 12; Ex. 2001, 31–32; Ex. 2002. Petitioner filed the Petition in this case more than one year later on March 7, 2022. Pet. 82. Patent Owner contends that the Petition is barred under § 315(b) because 2Wire and its successor-in-interest CommScope Holding Company, Inc. ("CommScope") are real parties in interest and privies of Petitioner.[1] Prelim. Resp. 23–28; Sur-reply 2–7.

1. Real Party in Interest

"Whether a party who is not a named participant in a given proceeding nonetheless constitutes a 'real party-in-interest' . . . to that proceeding is a highly fact-dependent question." Consolidated Trial Practice Guide, 13 (Nov. 2019), *available at* https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf ("TPG"). "[A]t a general level, the 'real party-in-interest' is the party that desires review of the patent," and, thus, "may be the petitioner itself, and/or it may be the party or parties at whose behest the petition has been filed." *Id.* at 14. "For example, a party that funds and directs and controls an IPR or PGR petition or proceeding constitutes a 'real party-in-interest.'" *Id.* at 17. Several relevant factors for determining whether a party is a real party in interest include the party's relationship with the petitioner, the party's relationship to the petition, and the nature of the entity filing the petition. *Id.* at 17–18.

[1] We do not address in this Decision whether 2Wire or CommScope is a real party in interest or privy of Petitioner for purposes of 35 U.S.C. § 315(e)(2). *See SharkNinja Operating LLC v. iRobot Corporation*, IPR2020-00734, Paper 11 at 19–20 (PTAB Oct. 6, 2020) (precedential).

Patent Owner argues that Petitioner filed the Petition at the behest of 2Wire and CommScope. Prelim. Resp. 26. Specifically, Patent Owner contends that Petitioner and CommScope are "'featured partner[s]' in business" who agreed to a "joint strategy." *Id.* at 27; Sur-reply 3–4. According to Patent Owner, Petitioner filed petitions challenging certain patents that 2Wire and CommScope are "unquestionably time barred from challenging," even though Petitioner is not accused of infringing them. Prelim. Resp. 25–27; Sur-reply 2–3. And, in "exchange," CommScope filed petitions challenging certain other patents that Petitioner is accused of infringing. Prelim. Resp. 27; Sur-reply 3. Patent Owner also contends that Petitioner and CommScope used the same declarants to support their respective petitions. Prelim. Resp. 27; Sur-reply 4.

On this record, we are not persuaded that Petitioner filed the Petition at the behest of 2Wire and CommScope. The evidence of record indicates that Patent Owner sent claim charts to Petitioner alleging infringement of the '381 patent based on compliance with Very High Speed Digital Subscriber Line ("VDSL") standards.[2] Reply 2; Ex. 1034, 37–38; Ex. 1035, 1–8; Ex. 1036, 1–8; Ex. 1037 ¶ 3. Although Patent Owner has not filed a complaint against Petitioner for infringement of the '381 patent, Patent Owner did file a complaint against Petitioner for infringement of another

[2] Petitioner argued in a related district court case that Patent Owner's communications do not provide a specific charge of infringement by a specific product that constitute actual notice under 35 U.S.C. § 287. Sur-reply 3–4; Ex. 2032, 11. Here, we rely on Patent Owner's communications only as evidence that Petitioner had its own interest in filing the Petition, not that those communications provided sufficient notice under § 287.

patent that includes similar claims. Ex. 1031, 5 ("asserts infringement of . . . United States Patent Nos. . . . 7,844,882"); *compare* Ex. 1001, 10:43–11:4, *with* IPR2022-00664, Ex. 1001, 11:39–12:12. Further, there is evidence that Patent Owner continues to demand that Petitioner "take a license to its entire portfolio," including the '381 patent. Reply 3 (emphasis omitted); Ex. 1037 ¶ 3. Thus, at this stage of the proceeding, the evidence of record indicates that Petitioner filed the Petition for itself, not at the behest of 2Wire and CommScope.

2. Privity

Whether a petitioner is in privity with another party "is a highly fact-dependent question." TPG, 13. Our "analysis seeks to determine whether the relationship between the purported 'privy' and the relevant other party is sufficiently close such that both should be bound by the trial outcome and related estoppels." *Id.* at 14–15. In *Taylor v. Sturgell*, 553 U.S. 880, 893–95 (2008), the Supreme Court provided "six categories" where nonparty preclusion may be found, namely 1) when "[a] person . . . agrees to be bound by the determination of issues in an action between others"; 2) "based on a variety of pre-existing 'substantive legal relationship[s]' between the person to be bound and a party to the judgment"; 3) when "a nonparty . . . was 'adequately represented by someone with the same interests who [wa]s a party'"; 4) when "a nonparty . . . 'assume[d] control' over the litigation in which [the] judgment was rendered"; 5) when a nonparty acts as "a proxy" to relitigate for a party; and 6) when "a special statutory scheme may 'expressly foreclos[e] successive litigation by nonlitigants.'" The Supreme Court noted, though, that this list

of six categories is just "a framework," not "a definitive taxonomy." *Id.* at 893 n.6.

Patent Owner argues that Petitioner had "a preexisting, established relationship" with CommScope. Prelim. Resp. 25. Specifically, Patent Owner contends that Petitioner and CommScope are "'featured partner[s]' in business." *Id.* at 27; Sur-reply 4–5. On this record, we are not persuaded by Patent Owner's argument. Under the second *Taylor* category, "[q]ualifying relationships include, but are not limited to, preceding and succeeding owners of property, bailee and bailor, and assignee and assignor." *Taylor*, 553 U.S. at 894. Patent Owner, though, does not identify any authority indicating that a business partnership alone is sufficient to find privity. *See* Prelim. Resp. 23–28; Sur-reply 2–7.

Patent Owner also argues that Petitioner filed the Petition as a "proxy" for 2Wire and CommScope. Prelim. Resp. 26. On this record, we are not persuaded by Patent Owner's argument. Patent Owner relies on the same alleged "joint strategy" discussed above. *Id.* at 25–27; Sur-reply 2–4; *see* Section II.D.1. For the same reasons discussed above, the evidence of record indicates that Petitioner filed the Petition for itself, not as a proxy for 2Wire and CommScope. *See* Section II.D.1.

E. Obviousness of Claims 1–8 over Mazzoni and VDSL1

Petitioner argues that claims 1–8 would have been obvious over Mazzoni and VDSL1. Pet. 11–51. For the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1–8 would have been obvious over Mazzoni and VDSL1.

1. Claim 1

Claim 1 recites "[a] non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver."[3] Ex. 1001, 10:43–46. Petitioner presents evidence that Mazzoni teaches a VDSL system with a memory that "can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Pet. 21–25 (citing Ex. 1005, 1:47–49, 1:59–65, 2:3–15, 2:57–58, 5:61–67) (emphases omitted); *see id.* at 35–36 (citing Ex. 1005, 5:21–27).

Patent Owner responds that Mazzoni does not teach a shared memory. Prelim. Resp. 42–44. Specifically, Patent Owner argues that "Mazzoni describes a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values." *Id.* at 42–43 (citing Ex. 1005, 3:62–4:14, 6:11–53). According to Patent Owner, "[t]here is no disclosure in Mazzoni that, once fixed at installation, any portion of the memory dedicated to the interleaver could ever be used by the deinterleaver and, conversely, that any portion of the memory dedicated to the deinterleaver could ever be used by the interleaver." *Id.* at 43.

On this record, Patent Owner's argument in unavailing. Mazzoni teaches that "parameters I, M, I' and M' . . . define the sizes of the respective

[3] We need not decide whether the preamble in any of the challenged independent claims is limiting because we determine that the prior art teaches the recitations in each preamble.

memory spaces assigned to the interleaving means and to the deinterleaving means." Ex. 1005, 5:21–27. As Patent Owner points out, Mazzoni teaches retrieving parameters I, M, I' and M' "[w]hen the modem is installed at the end of the line." *Id.* at 6:55–59. But Mazzoni also teaches that "parameters I, M, I' and M' can be *modified*, e.g., by software." *Id.* at 5:21–23 (emphasis added). In particular, Mazzoni's "memory allocation *can be reconfigured* in accordance with the bit rate actually processed by the send/receive device." *Id.* at 1:59–65 (emphasis added). Thus, the evidence of record indicates that Mazzoni's allocation of memory to the interleaver and deinterleaver is not fixed, but, rather, can be reconfigured according to the bit rate actually processed by the terminal.

Claim 1 recites "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver." Ex. 1001, 10:47–50. Petitioner presents evidence that Mazzoni teaches a VDSL system with a transceiver. Pet. 25–27 (citing Ex. 1005, 1:8–15, 1:60–61, 4:30–32, 6:6–8). Petitioner presents evidence that VDSL1 teaches a transceiver for transmitting an R-MSG2 message that specifies a maximum amount of memory available to be allocated to an interleaver. *Id.* at 27–30 (citing Ex. 1007, 13, 16, 20, 63, 77, 111, 132). As discussed in more detail below, Petitioner also presents evidence that it would have been obvious to combine the cited teachings of Mazzoni and VDSL1 so that Mazzoni's transceiver uses an initialization message to specify the maximum amount of memory available to be allocated to the interleaver. *Id.* at 16–21 (citing Ex. 1003 ¶¶ 77–84).

Patent Owner responds that VDSL1 does not teach a message specifying a maximum number of bytes of memory that are available to be allocated to an interleaver. Prelim. Resp. 52–53. Specifically, Patent Owner argues that "[t]he R-MSG2 and O-MSG2 messages provide the interleaver settings of each device," but "[t]here is no disclosure that these messages are tied to allocating any memory on any device or specifying a maximum number of bytes that could be allocated." *Id.* at 52.

On this record, Patent Owner's argument is unavailing. VDSL1 teaches that the R-MSG2 message includes a field specifying the "[m]aximum interleaver memory." Ex. 1007, 132. VDSL1 also includes a note indicating that the "[m]aximum interleaver memory" field is related to computing the amount of memory allocated to an interleaver. *Id.* ("Maximum interleaver memory . . . (see note 2) . . . NOTE 2: The interleaver memory is computed as M×I×(I-1)."). Thus, the evidence of record indicates that VDSL1's R-MSG2 message is related to allocating memory to an interleaver.

Claim 1 recites that the transceiver is capable of "determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." Ex. 1001, 10:51–54. Petitioner presents evidence that Mazzoni teaches determining the amount of memory required by the interleaver to interleave a first plurality of RS coded data bytes. Pet. 31–36 (citing Ex. 1003 ¶¶ 147–164; Ex. 1005, 4:38–43, 5:21–27, 6:11–48). Other than the arguments discussed above, at this stage of the proceeding, Patent Owner does not dispute that the Mazzoni and VDSL1 combination teaches this limitation of claim 1.

Claim 1 recites that the transceiver is capable of "allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message." Ex. 1001, 10:55–60. Petitioner presents evidence that Mazzoni teaches assigning memory space ESM1 to the interleaver. Pet. 37–39 (citing Ex. 1005, 5:21–27, 5:64–67). Petitioner presents evidence that VDSL1 teaches an R-MSG2 message that specifies a maximum amount of memory available to be allocated to an interleaver. *Id.* at 39–42 (citing Ex. 1007, 16, 111, 127, 129, 132). As discussed in more detail below, Petitioner also presents evidence that it would have been obvious to combine the cited teachings of Mazzoni and VDSL1 so that Mazzoni's transceiver uses an initialization message to specify the maximum amount of memory available to be allocated to the interleaver. *Id.* at 16–21 (citing Ex. 1003 ¶¶ 77–84). Other than the arguments discussed above, at this stage of the proceeding, Patent Owner does not dispute that the Mazzoni and VDSL1 combination teaches this limitation of claim 1.

Claim 1 recites that the transceiver is capable of "allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate." Ex. 1001, 10:61–64. Petitioner presents evidence that Mazzoni teaches assigning memory space ESM2 to a deinterleaver. Pet. 43 (citing Ex. 1005, 5:21–24, 5:64–67). Other than the arguments discussed above, at this stage of the proceeding, Patent Owner

does not dispute that the Mazzoni and VDSL1 combination teaches this limitation of claim 1.

Claim 1 recites that the transceiver is capable of "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver." Ex. 1001, 10:65–11:4. Petitioner presents evidence that Mazzoni teaches a dual-port random access memory, and a person of ordinary skill in the art would have known that a dual-port memory would allow the interleaver and deinterleaver to access their respective portions of the memory at the same time. Pet. 44–45 (citing Ex. 1003 ¶¶ 183–190; Ex. 1005, 5:61–67). Other than the arguments discussed above, at this stage of the proceeding, Patent Owner does not dispute that the Mazzoni and VDSL1 combination teaches this limitation of claim 1.

2. Claims 2–8

Independent claim 5 recites limitations similar to those discussed above for claim 1. Dependent claims 2–4 and 6–8 depend from claim 1 or 5. Petitioner presents evidence that the Mazzoni and VDSL1 combination teaches the limitations of claims 2–8. Pet. 46–51. Other than the arguments discussed above, at this stage of the proceeding, Patent Owner does not dispute that the Mazzoni and VDSL1 combination teaches the limitations of claims 2–8.

3. Reason to Combine

Petitioner argues that a person of ordinary skill in the art would have had reason to combine the cited teachings of Mazzoni and VDSL1. Pet. 16–21 (citing Ex. 1003 ¶¶ 77–84). In particular, Petitioner presents evidence that "Mazzoni contemplates a transceiver for sending/receiving digital data, 'in particular in a VDSL environment,'" and "VDSL1 is the technical specification put forth by ETSI that 'specifies requirements for . . .' VDSL." *Id.* at 16 (citing Ex. 1005; Ex. 1007, 9) (emphasis omitted). Petitioner presents evidence that a person of ordinary skill in the art "would have been motivated to combine the initialization protocols of VDSL1 with the transceivers disclosed by Mazzoni." *Id.* at 17 (citing Ex. 1003 ¶ 79). For example, according to Petitioner, a person of ordinary skill in the art "looking to build a functioning transceiver that operated in a VDSL environment would have sought to comply with the VDSL1 technical specification." *Id.* at 18 (citing Ex. 1003 ¶ 80).

Patent Owner responds that Petitioner does not show sufficiently that a person of ordinary skill in the art would have had reason to combine the cited teachings of Mazzoni and VDSL1. Prelim. Resp. 54–58. Specifically, Patent Owner argues that "[t]he total size of Mazzoni's memory . . . is fixed at 26,892 bytes," but "the R-MSG2 and O-MSG2 messages [in VDSL1] provide settings that require more than 26,892 bytes of memory." *Id.* at 56 (citing Ex. 1003 ¶ 155; Ex. 1005, 4:18–22, 6:45–50). According to Patent Owner, the O-MSG2 message "would include the settings for [service] A6," which requires "24,960 bytes" of interleaver memory, and the R-MSG2 message "would include the interleaver settings for [service] S6," which requires "10,920 bytes" of interleaver memory. *Id.* at 56–57 (citing

Ex. 1003 ¶ 156; Ex. 1005, 3:66–4:2, 5:19–30). Patent Owner concludes that "[a]pplying these settings in the contract would result in a total memory requirement at the [terminal] TU of 35,880 bytes," which is more than the "26,892 bytes of memory" available in Mazzoni. *Id.* at 57.

On this record, Patent Owner's argument is unavailing. Mazzoni explains that in a typical VDSL communication system, an operator can provide a user with a symmetrical service (e.g., services S1–S6) where the bit rates are the same in the uplink and downlink directions, or an asymmetrical service (e.g., services A1–A6) where the bit rates are different in the uplink and downlink directions. Ex. 1005, 3:62–4:14. Patent Owner's argument above is premised on a scenario where an operator terminal is configured for service A6, but a user terminal is configured for service S6. Prelim. Resp. 56–57. Patent Owner, though, does not identify specific evidence indicating that such a scenario would occur. *See id.* at 54–58. Rather, the evidence of record indicates that in Mazzoni and VDSL1, the operator and user are configured for the same VDSL service. Ex. 1005, 6:55–59 ("When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table."); Ex. 1007, 127 ("The VTU-O and VTU-R then enter an iterative procedure to agree on a contract for the transmission.").

4. Summary

For the foregoing reasons, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1–8 would have been obvious over Mazzoni and VDSL1.

F. Obviousness of Claims 1–8 over VDSL1 and Fadavi-Ardekani

Petitioner argues that claims 1–8 would have been obvious over VDSL1 and Fadavi-Ardekani. Pet. 51–72. Because we determined above that Petitioner demonstrates a reasonable likelihood of prevailing on the asserted ground based on Mazzoni and VDSL1, we also institute an *inter partes* review on the asserted ground based on VDSL1 and Fadavi-Ardekani. *See* TGP, 64. Nonetheless, we provide a preliminary analysis of the parties' arguments regarding the asserted ground based on VDSL1 and Fadavi-Ardekani "to provide guidance to the parties for the upcoming trial." *Id.*

Claims 1 and 5 recite a "shared memory." Ex. 1001, 10:53–54, 11:21–22. Petitioner argues that Fadavi-Ardekani's Interleave/De-Interleave Memory ("IDIM") is a shared memory where a portion of the memory can be used by either an interleaver or a deinterleaver. Pet. 62. Patent Owner responds that Fadavi-Ardekani does not teach a shared memory. Prelim. Resp. 44–50.

On this record, we agree with Patent Owner. Fadavi-Ardekani teaches that the IDIM "may be utilized in a ping-pang fashion." Ex. 1006, 6:55–58. Fadavi-Ardekani explains that

> [f]or example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory. Between the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.

Id. at 8:59–9:3. In other words, Fadavi-Ardekani's IDIM has one portion that is used as interleave memory and another portion that is used as deinterleave memory. *Id.* Although the DSP and FCI may alternately access those two portions of the IDIM, Fadavi-Ardekani does not appear to teach that the same portion of the IDIM can be used as either interleave memory or deinterleave memory. *See id.*

Petitioner argues that Fadavi-Ardekani's "optimal implementation" teaches a shared memory. Pet. 61. Specifically, Petitioner contends that

> Fadavi-Ardekani explains that the invention "*utilizes the same memory for receive data and transmit data*," and thus the interleaver/deinterleaver may be assigned only 16 Kbytes. Ex. 1006, 7:25-30. Because one ADSL session requires 16 Kbytes in the downstream and 2 Kbytes in the upstream—for a total of 18 Kbytes—and the RAM available to the interleaver/deinterleaver is only 16 Kbytes (after accounting for 4 Kbytes for the fast path buffer), a portion of the memory must be used by both the interleaver and deinterleaver to implement the disclosed session. Ex. 1003, ¶ 228.

Id. Petitioner appears to argue that the cited portion of Fadavi-Ardekani teaches using the same portion of the IDIM for both interleaving and deinterleaving during the same session. *Id.* But, at this stage of the proceeding, Petitioner's argument does not appear to be consistent with the evidence of record. *See* Ex. 1006, 8:59–9:3 (describing alternating access of an interleave portion and a deinterleave portion); Ex. 2014, 574:14–575:21 (discussing an alleged "error" in Petitioner's interpretation of Fadavi-Ardekani).

Alternatively, Petitioner argues that a person of ordinary skill in the art would have known to use a shared memory in Fadavi-Ardekani. Pet. 60–61. In particular, Petitioner contends that

> [a] POSA looking to Fadavi-Ardekani for a beneficial environment in which to implement VDSL would have understood that a dynamically allocable shared memory would be selected because support of both asymmetric and symmetric streams requires that the ratio of interleaver and deinterleaver sizes is *not fixed* and the flexibility to use a portion of the memory for interleaving or deinterleaving would necessarily be required to implement the full range of VDSL. Ex. 1006, 7:30-33; Ex. 1003, ¶ 227.

Id. Petitioner appears to argue that even if Fadavi-Ardekani does not teach a shared memory, a person of ordinary skill in the art would have known to use a shared memory. *Id.* Petitioner explains why using a shared memory would have been beneficial. *Id.* But Petitioner does not appear to identify specific evidence indicating that a shared memory was well known or otherwise would have been within the background knowledge of a person of ordinary skill in the art. *See id.*; Ex. 1003 ¶ 227; *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) ("[W]e have emphasized the importance of a factual foundation to support a party's claim about what one of ordinary skill in the relevant art would have known.").

Nonetheless, as discussed above, because we determine that Petitioner demonstrates a reasonable likelihood of prevailing on the asserted ground based on Mazzoni and VDSL1, we also institute an *inter partes* review on the asserted ground based on VDSL1 and Fadavi-Ardekani. Patent Owner may raise its arguments regarding the VDSL1 and Fadavi-Ardekani combination again in its response to the Petition after institution.

III. CONCLUSION

Petitioner demonstrates a reasonable likelihood of prevailing in showing the unpatentability of at least one of the challenged claims of the '381 patent. At this stage of the proceeding, we have not made a final

determination with respect to the patentability of any of the challenged claims.

IV. ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–8 of the '381 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '381 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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