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Paper 13
Date: May 12, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROCHIP TECHNOLOGY INC.,
Petitioner,

v.

HD SILICON SOLUTIONS LLC,
Patent Owner.

IPR2021-01420
Patent 7,260,731 B1

Before FRANCES L. IPPOLITO, NATHAN A. ENGELS, and ARTHUR M. PESLAK, *Administrative Patent Judges.*

ENGELS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Petitioner Microchip Technology, Inc. filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 1–7 of U.S. Patent No. 7,260,731 B1 (Ex. 1001). Patent Owner HD Silicon Solutions LLC filed a Preliminary Response. Paper 12 ("Prelim. Resp.").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition and any response thereto shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons explained below, upon considering the Petition, Preliminary Response, and evidence of record, we determine the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we do not institute *inter partes* review.

A. Real Parties in Interest

Petitioner identifies Microchip Technology Incorporated as the real party-in-interest. Pet. 1. Patent Owner identifies HD Silicon Solutions LLC as the real party-in-interest. Paper 4, 2.

B. Related Matters

The parties state that the '731 patent is the subject of *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 6:20-cv-01092 (W.D. Tex.). Pet. 1; Paper 4, 2. That case has been transferred to *HD Silicon Solutions LLC v. Microchip Technology Inc.*, No. 3:21-cv-08295-SK (N.D. Cal.). Paper 6, 2.

Petitioner additionally states that it filed Petitions in IPR2021-00752, IPR2021-00872, IPR2021-01042, IPR2021-01089, and IPR2021-01265. Pet. 2.

C. The '731 Patent

Titled "Saving Power When in or Transitioning to a Static Mode of a Processor," the '731 patent is directed to reducing power consumption of a computer system during intervals in which a processor is stopped. Ex. 1001, 1:7–11, codes (54), (57). The '731 patent states that typically a processor is stopped by terminating the system clocks furnished to the processor, putting the processor into a "deep sleep" state. Ex. 1001, 1:26–53. Maintaining that state requires application of a core voltage to various circuits, "which generates a power dissipation referred to in th[e] specification as 'static power' usage because the processor is in its static state in which clocks are disabled." Ex. 1001, 1:53–57. The '731 patent describes reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clocks are disabled thereby reducing the power used by the processor in the deep sleep state. Ex. 1001, 2:3–9, 3:18–22.

D. Illustrative Claims

Of the challenged claims, claims 1, 4, and 6 are independent claims. Claim 1, reproduced below, is illustrative.

> 1. A method for reducing power utilized by a processor comprising the steps of:
>
> determining that a processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled, and
>
> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which said system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor,
>
> responsive to said determining, at a voltage regulator supplying said core voltage, transitioning from a first regulation mode to a second regulation mode,

> wherein power is dissipated during a voltage transition that reduces said selectable voltage in said first regulation mode and power is saved during said voltage transition in said second regulation mode.

E. Alleged Grounds of Unpatentability

Petitioner asserts that claims 1–7 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
1, 3, 6, 7	103	NEC-Databook,[2] Burd[3]
2	103	NEC-Databook, Burd, Nguyen[4]
4, 5	103	NEC-Databook, TI-TPS5210-Datasheet,[5] Kikinis[6]

II. ANALYSIS

A. Level of Ordinary Skill in the Art

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom*

[1] Based on the '731 patent's filing date, we apply the pre-AIA version of § 103.
[2] Single-Chip Microcomputer Databook, NEC Electronics Inc. (May 1990). Ex. 1005 ("NEC-Databook").
[3] Thomas Burd et al., "A Dynamic Voltage Scaled Microprocessor System," Digest of Technical Papers, 2000 IEEE Int. Solid-State Circuits Conf. (Feb. 2000). Ex. 1006 ("Burd").
[4] US 5,955,871, Sept. 21, 1999. Ex. 1007 ("Nguyen").
[5] Texas Instruments, Inc., "TPS5210 Programmable Synchronous-Buck Regulator Controller," May 1999. Ex. 1008 ("TI-TPS5210-Datasheet").
[6] US 5,919,262, July 6, 1999. Ex. 1009 ("Kikinis").

Accessories, Inc. v. Jeffrey-Allan Indus., Inc., 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends a person of ordinary skill in the art at the time of the invention would have been a person with "at least a bachelor's degree in electrical engineering, computer engineering, or computer science, with at least two years of experience in computer system development, including experience developing power/voltage regulation systems for portable devices." Pet. 6. Petitioner also states that a person may qualify as a person of ordinary skill with more formal education and less experience or vice versa. Pet. 6 (citing Ex. 1002 ¶¶ 42–44, 45–89).

Patent Owner does not address the level of ordinary skill. For the purposes of this Decision, we adopt Petitioner's recitation of the level of ordinary skill.

B. Ground 1: NEC-Databook and Burd

The Petition includes a limitation-by-limitation comparison of the combination of NEC-Databook and Burd to claims 1, 3, 6, and 7. Pet. 24–53. Petitioner also presents arguments for combining NEC-Databook and Burd. Pet. 53–60.

For each of claims 1, 3, 6, and 7, Petitioner proposing combining the teachings of NEC-Databook and Burd's teachings of a prototype voltage regulator. Pet. 24–53. Specifically, discussing limitation 1[c], Petitioner's combination includes using the PTO0, PTO1, and PCL signals from the microcomputers disclosed in NEC-Databook to send a "new frequency request" to Burd's voltage regulator to reduce the core voltage supplied to the μPD751xx–CPU, causing the regulator to switch from one regulation mode to another. Pet. 35. Petitioner contends "[t]his transition would change the status of signals PTO0, PTO1, and/or PCL from a

changing/counting state to a stable state. This state change can be detected and used to present a 'new frequency request' of 28 MHz to Burd's regulator/controller, which corresponds to a voltage regulator output of approximately 2.0V," such that the μPD751xx-CPU would transition to Data Retention mode. Pet. 37. According to Petitioner, a person of ordinary skill would understand that "while supplying 3.8V, which corresponds to f_{CLK} of 80 Mhz, if a 'new frequency request' of 28 MHz is presented, F_{ERR} would be -52 Mhz, and Burd's regulator would transition from the 'regulation mode' (*first regulation mode*) to the 'tracking mode' (*second regulation mode*)." Pet. 38. Petitioner contends that "[s]uch a transition is shown in Burd's Figure 17.4.3, although with a voltage transition of 3.8 to 1.2 V, rather than the 3.8 to 2 V of this obviousness combination." Pet. 38.

Although not a requirement of claim 1, Petitioner's contentions regarding claim 3 provide further detail regarding how the proposed combination would perform the step of reducing core voltage. Pet. 44–46. Petitioner contends "Burd's digital loop filter would adjust the output voltage to approximately 2 V (the minimum data retention voltage for the μPD751xx-CPU . . . at a desired operating frequency of approximately 28 MHz." Pet. 45 (citing Ex. 1002 ¶ 304; Ex. 1005, 47, 64). Citing Dr. Alpert's Declaration, Petitioner further contends that "if the 7-bit value provided to Burd's 'Desired Freq Register' is that corresponding to 80 MHz, e.g., '1010000,' the converter would output $V_{DD} \approx 3.8$ V." Pet. 45 (citing Ex. 1002 ¶¶ 220–221). Petitioner further contends that "if the 7-bit value provided to the 'Desired Freq Register' is that corresponding to 28 MHz, e.g., '0011100,' Burd's digital loop filter would cause the regulator/converter to lower its output to approximately 2.0 B." Pet. 45–46 (citing Ex. 1002 ¶ 221).

One problem with Petitioner's contentions, though, is that Burd's regulator generates clock frequencies in the range of 28–80 MHz when outputting voltages from 2 to 3.8 V, while the NEC-Databook teaches a maximum speed of 4.19 MHz. Pet. 55 (citing Ex. 1002 ¶¶ 210–226; Ex. 1005, 35). According to Petitioner, "[w]hile Burd suggests that F_{CLK} may also be used to clock a processor, a [person of ordinary skill] would have understood that *a separate clock generation system could* be used to clock the processor." Pet. 55 (emphasis added). Dr. Alpert states that to accommodate a separate clock generation system in the proposed combination, "Burd's system can be modified merely to disconnect or eliminate the clock buffer supplying a clock signal generated by the 'Ring Oscillator' to the CPU." Ex. 1002 ¶ 223; *accord* Pet. 56. According to Petitioner, a person of ordinary skill "would have recognized this modification of Burd's regulator ('*voltage regulator*') to be straightforward, as nothing more than eliminating a circuitry component and an associated path, and providing *certain binary values* as required, which are circuitry configuration activities that a [person of ordinary skill] would have routinely performed." Pet. 57 (citing Ex. 1002 ¶ 226) (emphasis added).

Among other problems with the Petition's arguments, Petitioner does not explain what "certain binary values" would be provided or how those binary values would supply the 7-bit values required by Burd's "Desired Freq Register." *See* Pet. 44–46, 57; Prelim. Resp. 34–35, 38–39. Moreover, Petitioner states in its arguments for Ground 2 that a person of ordinary skill would have recognized that without an adjustable voltage regulator that can adjust voltage based on workload, the µPD751xx-CPU's "potential of power/energy saving would not materialize" (Pet. 89 (citing Ex. 1002 ¶ 352)), yet Petitioner's proposed combination for Ground 1 would provide

only one operating voltage, along with a sleep state voltage (Pet. 38 (stating Burd's regulator would supply 3.8 V and 2.0 V)).

In sum, neither Petitioner nor Dr. Alpert adequately explains why a person of ordinary skill would have been motivated to make the proposed modifications without improper hindsight. It is not enough that a person of ordinary skill *could* theoretically combine the teachings of two references; particularly in view of the modifications required, Petitioner has not established that a person of ordinary skill, as defined by Petitioner, would have had reason to combine NEC-Databook and Burd to arrive claim 1. The same problems exist in Petitioner's proposed combination for claims 3, 6, and 7. Accordingly, Petitioner has not shown a reasonable likelihood that it would prevail with respect to claims 1, 3, 6, or 7 as challenged in Ground 1.

C. Ground 2: NEC-Databook, Bard, and Nguyen

Building on Petitioner's showings for independent claim 1, the Petition includes a comparison of dependent claim 2 to the combined teachings of NEC-Databook, Bard, and Nguyen, with Nguyen cited only for the limitations added by claim 2. Pet. 60. Because Petitioner relies on the same reasons for combining NEC-Databook and Burd (Pet. 63 ("The motivation to combine NEC-Databook and Burd is discussed above in Ground 1.")) and does not rectify the deficiencies discussed above (*see* Pet. 63–65), Petitioner has not adequately shown reasons to combine the references to arrive at claim 2. Accordingly, Petitioner has not shown a reasonable likelihood that it would prevail with respect to claim 2 as challenged in Ground 1.

D. Ground 3: NEC-Databook, TI-TPS5210-Datasheet, and Kikinis

The Petition includes a limitation-by-limitation comparison of claims 4 and 5 to the combined teachings of NEC-Databook, TI-TPS5210-

Datasheet, and Kikinis. Pet. 66–86. Petitioner also provides a number of arguments for combining the references. Pet. 86–91.

For both of claims 4 and 5, Petitioner proposes combining NEC-Databook's μPD751xx microcontroller, the TPS5210-Datasheet's regulator, and Kinikis's R-ladder circuitry. *See*, *e.g.*, Pet. 91. Specifically, Petitioner contends "TI-TPS5210-Datasheet discloses furnishing inputs VID0-VID4 to reduce the TPS5210 regulator's output voltage, which may be supplied as core voltage to NEC-Databook's μPD751xx-CPU." Pet. 67 (citing Ex. 1002 ¶ 361). Petitioner contends a person of ordinary skill would have understood that Kikinis's R-ladder could replace one of TI-TPS5210-Datasheet's resistors and that the NEC-Databook 's PTO0, PTO1, and/or PCL signals controlling the R-ladder based on whether the μPD751xx-CPU is in the Operation or STOP mode. Pet. 71. According to Petitioner, NEC-Databook 's PTO0, PTO1, and PCL signals are functionally equivalent to Kikinis's "early warning signals" supplied as inputs to its voltage regulator.

Kikinis teaches that the early warning signals indicate that its processor is about to wake up from a sleep state based on a wake-up mechanism which receives signals in interrupt lines to its CPU. Ex. 1009 3:6–14, Fig. 5. According to Kikinis, the wake-up mechanism provides the early warning signals as part of a scheme "to reduce or eliminate the capacitors required to deal with the current surge that occurs when the CPU goes from idle (typically in the milliamp range) to active (typically in a range of multiple amperes). Ex. 1009 3:1–5. In contrast, NEC Datasheet's PTO0, PTO1, and PCL signals relate to a transition to the STOP mode and are generated by the timer/event counter output pins and clock output pins. Ex. 1005, 29. NEC Datasheet does not concern reducing or eliminating capacitors, and it is not clear how Petitioner contends a person of ordinary

skill would have selected Kikinis's teachings and replaced its wake-up mechanism with the input signals from NEC Datasheet to control Kikinis's R-ladder. Throughout its discussion of rationales for combining the references, Petitioner provides conclusory statements regarding what a person of ordinary skill "would have understood," citing the Alpert Declaration which merely mirrors the Petition with largely the same conclusory statements, along with a laundry list of rationales that mirror the language of *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007). Pet. 86–90. Based on the evidence currently of record, however, we determine Petitioner's has not adequately supported a rationale for its proposed combination of the references, as Petitioner's combination is guided by improper hindsight rather than rationale underpinnings. Accordingly, we determine Petitioner has not shown a reasonable likelihood that it would prevail in its challenge to claims 4 and 5 in Ground 3.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has not demonstrated a reasonable likelihood that it will prevail with respect to at least one claim of the '731 patent. Accordingly, we do not institute *inter partes* review. Because we deny institution on the merits, we do not reach the parties' arguments regarding discretionary denial under 35 U.S.C. § 314(a).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that pursuant to 35 U.S.C. § 314(a), the Petition for institution of *inter partes* review of claims 1–5 of U.S. Patent No. 7,260,731 is denied.

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