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Paper 52
Date: April 13, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.
Petitioner,

v.

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Patent Owner.

IPR2020-01596
Patent 7,187,709 B1

Before JOHN F. HORVATH, DANIEL J. GALLIGAN and RUSSELL E. CASS, *Administrative Patent Judges.*

HORVATH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
Granting-in-Part Patent Owner's Motion to Exclude
35 U.S.C. § 318(a), 37 C.F.R. § 42.64(c)

I. INTRODUCTION

A. Background and Summary

Analog Devices, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–17 ("the challenged claims") of U.S. Patent No. 7,187,709 B1 (Ex. 1001, "the '709 patent"). Paper 3 ("Pet."), 26. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). Upon consideration of the Petition and Preliminary Response, we instituted *inter partes* review of all challenged claims on all grounds raised. Paper 12 ("Dec. Inst."), 49.

Patent Owner filed a Response to the Petition (Paper 26, "PO Resp."), Petitioner filed a Reply (Paper 32, "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 37, "PO Sur-Reply"). An oral hearing was held on January 11, 2022, and the hearing transcript is included in the record. *See* Paper 47 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(b). This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has demonstrated by a preponderance of evidence that claims 1–5, 8–12, and 15–17 of the '709 patent are unpatentable but has failed to demonstrate by a preponderance of evidence that claims 6, 7, 13, and 14 of the '709 patent are unpatentable.

B. Real Parties-in-Interest

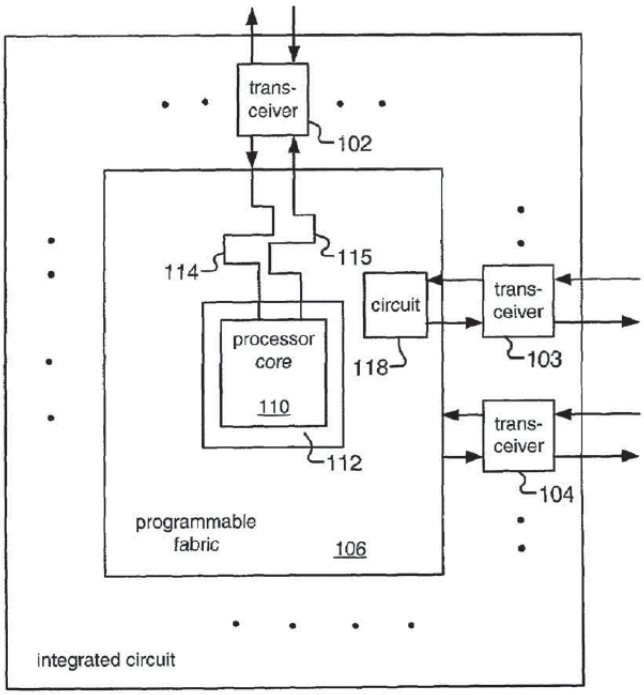
Petitioner identifies itself as the real party-in-interest. Pet. 1. Patent Owner identifies Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. as the real parties-in-interest. Paper 4 § A.

C. Related Matters

The parties identify the following as a related district court matter: *Analog Devices, Inc. v. Xilinx, Inc.*, No. 1:19-cv-02225 (D. Del.) ("the related District Court case"). Pet. 2; Paper 4 § B.

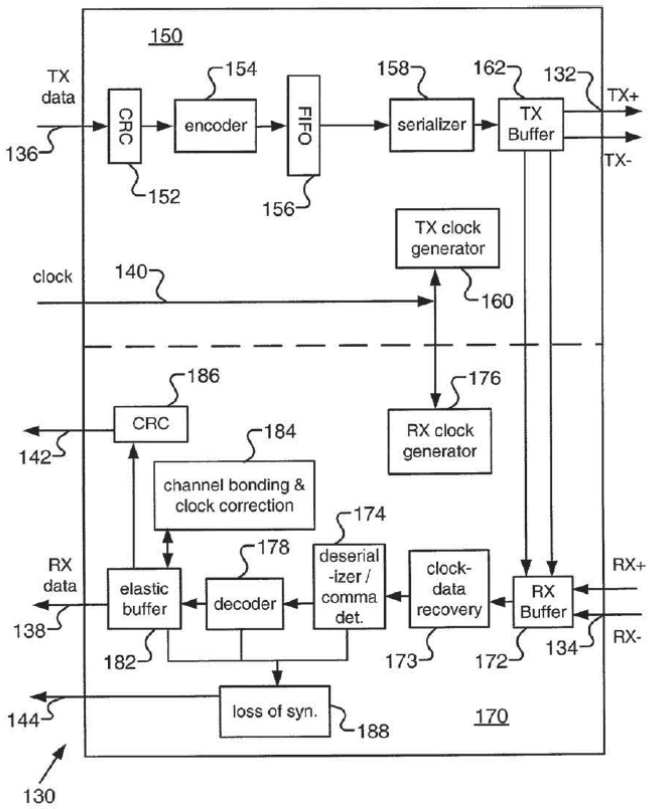
D. The '709 Patent

The '709 patent is directed to "an integrated circuit [IC] that contains a programmable fabric and a plurality of configurable transceivers located at the peripher[y] of the programmable fabric." Ex. 1001, 1:35–37. The IC "may contain one or more processor cores," and "[t]he processor core[s] and the transceivers can be connected by a plurality of signal paths that pass through the programmable fabric." *Id.* at 1:38–41. The IC can contain "a plurality of configuration memory cells," some of which "are associated with the programmable fabric while the others are associated with the configurable transceivers." *Id.* at 1:42–45. Such a circuit is shown in Figure 1 of the '709 patent, which is reproduced below.



The figure above is a schematic diagram of the invention disclosed in the '709 patent. *Id.* at 1:54–55. The IC includes transceivers 102–104, programmable fabric 106, and processor core 110. *Id.* at 1:64–2:4. Programmable fabric 106 can be a field programmable gate array (FPGA) fabric and "is intended for implementation of arbitrary logic functions" defined by users. *Id.* at 2:1–2, 2:46–49. Processor core 110 and transceiver 102 can be connected by signal paths 114/115 through programmable fabric 106. *Id.* at 2:10–14. The configuration memory cells can be used to "configure a plurality of circuits in programmable fabric 106," such as circuit 118, and "to configure the transceivers." *Id.* at 2:21–22, 2:38–40.

Figure 3 of the '709 patent, reproduced below, is a block diagram of a transceiver 130 used in the IC of Figure 1. *Id.* at 1:58–59.



The figure above is a block diagram of transceiver 130. *Id.* On transmit side 150, transceiver 130 includes CRC (cyclic redundancy code) generator 152, encoder 154, serializer 158, and transmit buffer 162. *Id.* at 3:36–4:44. CRC generator 152 can be configured to (a) be bypassed, (b) use a value to corrupt the CRC computation, (c) support different transmission standards (e.g., Fibre Channel and Gigabit Ethernet), and (d) use user-defined start-of-packet and end-of-packet control characters. *Id.* at 3:43–54. Encoder 154 is an 8B/10B encoder, and can be configured to (a) be bypassed and (b) modify the maintenance of the running disparity. *Id.* at 3:62–4:14. Serializer 158 multiplexes parallel data to a serial data stream, and can be configured to multiplex and transmit 10 or 20 bits per reference clock cycle. *Id.* at 4:31–38.

On receive side 170, transceiver 130 includes receive buffer 172, clock and data recovery 173, deserializer 174, decoder 178, elastic buffer 182, CRC verification 186, and loss of synchronization (LOS) detector 188. *Id.* at 4:45–6:12. Deserializer 174 can be configured to (a) receive 10 or 20 bits per clock cycle, (b) detect 8B/10B "plus" or "minus" comma patterns or alternative comma patterns, (c) raise a comma detect flag and/or realign byte boundaries upon detecting "plus," "minus," both, or neither comma pattern, and (d) force comma alignment on half-word boundaries. *Id.* at 4:55–5:10. Decoder 178 can be configured to (a) be bypassed and (b) raise a comma flag on "plus," "minus," both, or neither type of comma. *Id.* at 5:11–22. Elastic buffer 182 can be configured to (a) be bypassed, (b) use or inhibit clock correction, (c) set thresholds for flagging buffer overflows and underflows, and (d) select channel bonding modes, the number of channel bonding sequences, the lengths of matching byte values, and clock correction sequences. *Id.* at 5:23–40. CRC verification 186 can be

configured to (a) be bypassed, (b) support different transmission standards (e.g., Fibre Channel or Gigabit Ethernet), and (c) use user-defined start-of-packet and end-of-packet control characters. *Id.* at 5:51–60. LOS detector 188 can be configured to (a) be bypassed, (b) set the number of invalid characters needed to assert loss of synchronization, and (c) set the number of valid characters needed to decrement the count of invalid characters. *Id.* at 5:66–6:7.

E. Illustrative Claim

Claim 1 is illustrative of the challenged claims and is reproduced below.

> 1. An integrated circuit comprising:
>
> a plurality of configuration memory cells;
>
> programmable fabric circuitry coupled to the plurality of configuration memory cells, wherein the plurality of configuration memory cells are programmable to implement a circuit in the programmable fabric circuitry;
>
> a plurality of transceivers containing respective components having selectable values, said components being configured by said plurality of configuration memory cells, wherein one of said components is a loss of synchronization detector;
>
> wherein each configurable transceiver includes a configurable serializer and a configurable deserializer coupled to at least one of the configuration memory cells, wherein each serializer is configurable to transmit data at a selected bit rate, and each deserializer is configurable to receive data at the selected bit rate;
>
> wherein each transceiver has an input port that receives differential input signals and an output port that outputs differential output signals; and
>
> a plurality of signal paths coupling each configurable transceiver to a circuit implemented in the programmable fabric

circuitry, at least a portion of each of said signal paths passing through said programmable fabric circuitry.

Ex. 1001, 6:25–51.

F. Evidence[1]

Reference		Effective Date	Exhibit
Ralph D. Wittig and Paul Chow, *OneChip: An FPGA Processor With Reconfigurable Logic*, 1996 Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 17–19, 1996		Jan. 9, 1997[2]	1004
ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver, Preliminary Data Sheet, Lucent Technologies (Sept. 2000) ("ORT8850")		At least by Nov. 2000[3]	1005
Chan	US 6,542,096 B2	Apr. 1, 2003	1006
QL80FC – QuickFC™, Quicklogic QL80FC Programmable Fibre Channel ENDEC ("QL80FC")[4]			1008

[1] Petitioner also relies on the Declarations of Dr. Brent E. Nelson (Exs. 1003, 1030); Patent Owner relies on the Declaration of Michael C. Brogioli, Ph.D. (Ex. 2013).
[2] Petitioner relies on the Declarations of Sylvia Hall-Ellis (Ex. 1017 ¶¶ 46–55) and Gerard P. Grenier (Ex. 1016, ¶¶ 8–11) to establish the public availability of *OneChip*.
[3] Petitioner relies on the Declaration of Barry K. Britton to establish the public availability of *ORT8850*. *See* Ex. 1018 ¶¶ 10–21.
[4] For the reasons discussed in § II.A.3, *infra*, Petitioner fails to demonstrate the authenticity or public availability of this document.

G. Asserted Grounds

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Claims	35 U.S.C. §	References
1–5, 8–12, 15–17	103(a)	OneChip, ORT8850[5]
1–5, 8–12, 15–17	103(a)	Chan, ORT8850, OneChip
1–3, 6–8, 10, 13, 14, 17	103(a)	OneChip, ORT8850, QL80FC[6]
1–3, 6–8, 10, 13, 14, 17	103(a)	Chan, ORT8850, QL80FC, OneChip

II. ANALYSIS

A. Patent Owner's Motion to Exclude

Patent Owner filed a Motion to Exclude ORT8850 (Ex. 1005), QL80FC (Ex. 1008), Bursky (Ex. 1012), the Declaration of Sylvia Hall-Ellis, Ph.D. (Ex. 1033), and portions of the Affidavit of Elizabeth Rosenberg (Ex. 1019) and the Declaration of Barry K. Britton (Ex. 1018). Paper 42 ("Mot."), 1. Petitioner opposed the Motion (Paper 43, "Opp."), and Patent Owner replied (Paper 44, "Mot. Reply"). The Board decides evidentiary issues based on the Federal Rules of Evidence ("FRE"). 37 C.F.R. § 42.62(a). Patent Owner, as the movant, "has the burden of proof to

[5] Petitioner identifies this ground as obviousness over "OneChip in combination with ORT8850 and in view of Bursky." Pet. 12. As discussed *infra*, Petitioner relies on Bursky (Ex. 1012), in part, to demonstrate industry trends motivating the combination of OneChip and ORT8850. *See* Pet. 23–28. However, because Petitioner provides other reasons for the combination, we consider Petitioner's challenge to be based on the combination of OneChip and ORT8850. *Id.*

[6] Petitioner identifies this ground as obviousness over "OneChip in combination with ORT8850 and QL80FC in view of Bursky." Pet. 12. For the reasons discussed in n.5, *supra*, we consider Petitioner's challenge to be based on the combination of OneChip, ORT8850, and QL80FC.

establish that it is entitled to the requested relief." *Id.* § 42.20(c). For the reasons discussed below, we *grant-in-part* Patent Owner's motion to exclude.

1. Bursky and the Hall-Ellis Declaration

In our Institution Decision, we questioned whether Petitioner would "be able to sufficiently establish" the public availability of Bursky because no evidence for it was provided in the Petition. Dec. Inst. 16–18. Patent Owner asks us to confirm that preliminary finding. PO Resp. 27. Petitioner provides the Declaration of Sylvia Hall-Ellis, PhD. as supplemental evidence of Bursky's public availability. Pet. Reply 20 (citing Ex. 1033 ¶¶ 46–47). Patent Owner argues that Dr. Hall-Ellis's declaration should be excluded as untimely and Bursky's disclosures should be excluded as hearsay. *See* Mot. 15; PO Sur-Reply 22. Petitioner argues Dr. Hall-Ellis's declaration is timely filed in response to challenges raised in both the Institution Decision and Patent Owner's Response. Opp. 12–13 (citing CTPG[7] 73–74). Petitioner further argues that Bursky is self-authenticating under FRE 902(6), not hearsay, and not excludable under FRE 703 because Dr. Nelson relied on it in forming his opinion. Opp. 10–12. Patent Owner maintains that Bursky is hearsay and FRE 703 does not prohibit its exclusion. Mot. Reply 4–5.

Upon consideration of the evidence and arguments presented by the parties, we dismiss Patent Owner's motion to exclude Bursky and Dr. Hall-Ellis's declaration as moot. Although Petitioner identifies Bursky in Grounds 1 and 3, Petitioner does not rely on Bursky to teach any limitation in any of the claims challenged in Grounds 1 and 3. *See* Pet. 12, 28–60, 80–

[7] Consolidated Trial Practice Guide (Nov. 2019). Available at https://www.uspto.gov/TrialPracticeGuideConsolidated.

94. Instead, Petitioner relies on Bursky, in part, to support Dr. Nelson's testimony that combining the teachings of OneChip and ORT8850 would have been "consistent with literature at the time" of the invention because:

> industry was already disclosing or suggesting increased intergration of functionality—first by the integration of processor cores on programmable devices, and then by the integration of configurable, multi-protocol transceivers—to leverage the greater number of transistors available on an integrated device, and to satisfy the marketplace's desire for increased integration and reduction of cost.

Id. at 24–25 (citing Ex. 1003 ¶ 42). For example, Dr. Nelson testifies that Bursky reported "transceivers with configurable serializers/deserializers . . . [that] were integrated into programmable logic devices." Ex. 1003 ¶ 46. Dr. Nelson testifies that Bursky was published in Electronic Design Magazine, a trade periodical that a person skilled in the art "would have had access to and would have read to understand trends, such as the industry movement to SoC [System on a Chip] ongoing in the years before the '709 patent." Ex. 1030 ¶ 19.

In § II.D.3, *infra,* we do not rely on Bursky for providing a reason to combine the teachings of OneChip and ORT8850. Instead, we rely on Dr. Nelson's testimony and the teachings of the references themselves. Under FRE 703, Dr. Nelson's testimony is admissible even if Bursky is not. *See* Fed.R.Evid. 703 (allowing expert opinion based on facts or data "of a type reasonably relied upon by experts in the particular field" even if the facts or data are not admissible).

Accordingly, for the reasons discussed above, we need not determine the admissibility of Bursky or the Hall-Ellis declaration, and dismiss Patent Owner's motion to exclude them as moot.

2. ORT8850 and the Britton Declaration

Petitioner contends that ORT8850 (Ex. 1005) is a September 2000 data sheet that was publicly accessible by November 10, 2000, and submits the declaration of Barry K. Britton (Ex. 1018) in support of its contention. Pet. 22 (citing Ex. 1005, 1; Ex. 1018).

a) The Britton Declaration

Patent Owner argues that Exhibits A–J of the Britton declaration should be excluded for lack of authentication and as hearsay under FREs 801 and 802, and that paragraphs 4, 5, 10–15, 17–20, and 22 of the Britton declaration, which discuss Exhibits A–J, should also be excluded as hearsay. Mot. 10–13. Patent Owner argues that because "Mr. Britton lacks personal knowledge of his declaration's exhibits or how they were created, he cannot authenticate them." *Id.* at 12. Patent Owner next argues that because Mr. Britton relies on the dates printed on Exhibits A–D and J for the truth of the matter asserted, these Exhibits and paragraphs 4, 5, 10–15 and 17 of his declaration should be excluded as hearsay. *Id.* at 12–13. Patent Owner further argues that because Mr. Britton testified that he did not completely recognize Exhibit F, it and paragraphs 19 and 20 of his declaration should be excluded as hearsay. *Id.* at 13. Patent Owner argues Exhibit E should be excluded for the same reasons as ORT8850 (Ex. 1005). *Id.* Finally, Patent Owner argues that because Mr. Britton offered no testimony or opinion on the provenance of Exhibits G–I, they and paragraph 22 of his declaration should be excluded. *Id.*

Petitioner replies that Mr. Britton is a witness with knowledge who has authenticated Exhibits A–E and G–I because he recognized them and that the contents of these Exhibits are not hearsay because they fall under the business record and residual exceptions to the hearsay rule. Opp. 9–10.

Patent Owner maintains that Mr. Britton lacks personal knowledge to authenticate Exhibits A–J and that, by not addressing Exhibits F and J in its Opposition, Petitioner has conceded they are not authentic. Mot. Reply 3–4.

Upon considering all of the evidence and the arguments presented by the parties, we find Exhibits A–D, F, and J of the Britton declaration are authentic, and their contents are not hearsay. First, Exhibits B–D, F, and J are archived copies of Lucent webpages and documents captured at various times by the Wayback Machine. They are, therefore, inherently reliable. *See Valve Corp. v. Ironburg Inventions Ltd.*, 8 F.4th 1364, 1374–75 (Fed. Cir. 2021) ("District courts have taken judicial notice of the contents of webpages available through the Wayback Machine as facts that can be accurately and readily determined from sources whose accuracy cannot reasonably be questioned.") (internal quotation and citations omitted). To the extent that there is any dispute that these Exhibits are authentic Wayback Machine documents, we have confirmed that they are by direct comparison with documents obtained from the Wayback Machine via the links in Mr. Britton's declaration.[8] *See* Fed.R.Evid. 901(b)(3). Moreover, given the inherent reliability of the Wayback Machine, we find Exhibits B–D, F, and J are not only authentic copies of Wayback Machine documents, but also authentic copies of the Lucent webpages and documents Mr. Britton declares them to be.

[8] We note Mr. Britton filed an identical declaration with identical exhibits in a related proceeding. *See Analog Devices, Inc. v. Xilinx, Inc. and Xilinx Asia Pacific PTE., LTD*, IPR2020-01599, Ex. 1007. In that proceeding, a custodian of the Internet Archive identified exhibits B–D, F and J as "true and accurate copies" of webpages that had been captured and stored by the Internet Archive. IPR2020-01599, Ex. 1008 ¶¶ 1–6, pp. 5–26.

Second, Mr. Britton declares that in June 2000 he was the Senior Strategic Marketing Manager in the Network and Communications Core Group at Lucent, was aware of the types of technical documents Lucent made available on its customer-facing website describing the ORCA family of products (including the ORT8850 FPSC), and was aware of Lucent's standard practices for publishing and storing such documents. Ex. 1018 ¶¶ 4, 7–9. During cross-examination, he testified that he "would have been the person in charge of rolling that device [ORT8850 FPSC] out at that time," would have "done the press releases and the public documentation," and would have been "responsible for making sure they all got up on the web or got into customer's hands, into a data book . . . that type of thing." Ex. 2011, 8:19–22, 29:18–20. Although he did not personally upload the ORT8850 documentation to Lucent's website, he testified that his practice today is that "every three months or so I go get every document that we download . . . . So I would have done that at that time as well. I would have checked it." *Id.* at 47:16–25. He also testifies that he would have read all of the Application Notes, Data Sheets, and Product Briefs "that are related to the ORCA product line." *Id.* at 31:10–14.

On re-direct, regarding ORCA and ORT8850 documentation, Mr. Britton testified that he "would have had the responsibility for owning what - - not only what was published, but making sure it was published." *Id.* at 71:12–15. Mr. Britton further testified that he had reviewed his declaration and the Exhibits attached to it, prior to signing, and had "tried to make sure it was clear that I - - I had seen the webpages that w[ere] being reviewed that I - - I was signing off on was the webpage. I definitely remember that at the time of the press release and the time of the Data Sheet." *Id.* at 72:1–7.

Regarding specific archived webpages, Mr. Britton testified that he recognized Exhibit A as "the press release. I had written the press release and was quoted in that press release." *Id.* at 15:10–13. He testified that Exhibit C "would have been the top of the ORCA page on the external website" and that he was "definitely sure I clicked on that in the 2000s" in order "to see where the press release was and - - and the Data Sheet was." *Id.* at 41:6–14, 42:20–43:6. Regarding Exhibit D he testified that it "would have definitely been one of the pages I would have been responsible for." *Id.* at 44:23–24. Regarding Exhibit F, he testified that although he did not completely recognize it, he recognized the documentation it contained and that it was not a webpage "the customer would have seen" but was more of a "directory structure," such that "customer-facing webpage's link to here." *Id.* at 30:14–21, 31:22–32:9.

We find the totality of the evidence, discussed above, sufficient to also authenticate Exhibits A–D of Mr. Britton's declaration under FRE 901(b)(1) because Mr. Britton is a witness with knowledge of these Exhibits. As noted above, we find Exhibits B–D, F, and J are authentic copies of Lucent's webpages archived by the Wayback Machine. We further find the contents of Exhibits A–D, F, and J are not hearsay under FRE 803(6) because Mr. Britton is a qualified witness who has testified that they are records of a regularly conducted business activity. Because we do not rely on Exhibits G–I[9] for any reason, we dismiss as moot Patent Owner motion to exclude these Exhibits and paragraph 22 of the Britton declaration.

[9] We note that Exhibit I is a 112 page data sheet for the ORT8850 FPSC dated August 2001. *See* Ex. 1018, Ex. I. We further note that Patent Owner submitted the first 54 pages of this data sheet in an Information Disclosure Statement filed on Oct. 18, 2004. *See* Ex. 1002, 128; *see also* Ex. 2002.

For the reasons discussed above, we deny Patent Owner's motion to exclude Exhibits A–D, F, and J and paragraphs 4, 5, 10–14, and 17–20 of the Britton declaration as hearsay or for lack of authentication, and dismiss as moot Patent Owner's motion to exclude Exhibits G–I and paragraph 22 of the Britton declaration.

b) ORT8850

Patent Owner argues that ORT8850 should be excluded under FRE 901 for lack of authentication, and that Exhibit E of the Britton declaration should be excluded for the same reasons because "the two documents are identical." Mot. 5–10, 13; PO Resp. 27–31; PO Sur-Reply 19–22. Patent Owner argues Petitioner's counsel "supplied all of the exhibits to Mr. Britton's declaration" but provided "no evidence explaining the source of Exhibit 1005." Mot. 7. Therefore, Patent Owner argues, Mr. Britton cannot authenticate Ex. 1005 (ORT8850) because "he lacks specific, personal knowledge of ***this exhibit*****,** as opposed to the general practices of his former employer." *Id.* at 6. Patent Owner further argues that although the archived webpages for Lucent's ORCA product line have "hyperlinks to a data sheet for the ORT8850 device," the webpages "do not show that ***Exhibit 1005*** corresponds to those links—especially as all of the relevant hyperlinks are non-operational and defunct." *Id.* at 8–9. Patent Owner also questions

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Patent Owner has previously argued that "the two versions of ORT8850," i.e., the September 2000 version (Ex. 1005) and the partial August 2001 version (Ex. 2002) "are not materially different." Prelim. Resp. 17 (emphasis omitted). We find Patent Owner's admission and the substantial similarity between Exhibit 1005 (September 2000 data sheet) and Exhibit I of the Britton declaration (entire August 2001 data sheet) to be further evidence that Exhibit 1005 and Exhibit E of the Britton declaration are what Petitioner purports them to be – a September 2000 data sheet for the ORT8850 FPSC.

whether Mr. Britton's declaration "accurately and reliably reflects his knowledge of Lucent's actual practices" because "Petitioner's attorneys drafted his declaration." *Id.* at 9. Finally, Patent Owner argues the date printed on Exhibit 1005 is hearsay, and should be excluded. *Id.* at 10.

Petitioner replies that "Mr. Britton is more than qualified to authenticate Ex. 1005, the ORT8850 Data Sheet, pursuant to FRE 901(b)(1)" and that "his testimony ***alone*** is sufficient to authenticate the document" under that rule. Opp. 3, 5. Petitioner further argues that ORT8850 is "separately admissible under FRE 901(b)(4) and 902(7)" because it "bears the name 'Lucent Technologies' as well as that company's label, and follows the format of other Lucent Data Sheets, including its title and label as 'Preliminary Data Sheet.'" *Id.* at 3–4. Finally, Petitioner argues that although it doesn't rely only the date printed on the face of ORT8850, that date is not hearsay because it falls under FREs 803(6) and 807, the business records and residual exceptions to the hearsay rule. *Id.* at 8–9.

Patent Owner maintains that Mr. Britton's "general recollection of Lucent's website and practices do not establish that the alleged version submitted as Exhibit 1005 was publicly available in late 2000." Mot. Reply 2. Patent Owner further argues that at most FRE 901(b)(4) "might confirm that ORT8850 resembles publicly available data sheets—not that OR[T]8850 was itself factually public[ly] available." *Id.* Patent Owner also argues that FRE 902(7) cannot authenticate ORT8850 because "it merely authenticates '[a]n inscription, sign, tag, or label' on a document, not the document to which it is attached." *Id.* (quoting Fed.R.Evid. 902(7)).

Upon considering all of the evidence and the arguments presented by the parties, we find ORT8850 and Exhibit E of the Britton declaration are authentic and their content is not hearsay. Regarding Lucent's ORCA

product line, Mr. Britton testified on cross-examination that he was familiar with its documentation and that he would have read all of the Application Notes, Data Sheets, and Product Briefs "that are related to the ORCA product line." *Id.* at 31:10–14. Regarding the ORT8850 FPSC in particular, Mr. Britton testified that he "would have been the person in charge of rolling that device out at that time," would have "done the press releases and the public documentation," and would have been "responsible for making sure they all got up on the web or got into customer's hands, into a data book . . . that type of thing." Ex. 2011, 8:19–22, 29:18–20. He further testified that although he did not personally upload ORT8850 documentation to Lucent's website, his practice today is to download documentation he is responsible for publishing on the web "every three months or so" and that he "would have done that at that time as well. I would have checked it." *Id.* at 47:16–48:7. On re-direct, he testified that he "had the responsibility for owning what - - not only what was published, but making sure it was published. That was . . . specifically my responsibility at that time." *Id.* at 71:12–15.

Regarding Exhibit E of his declaration—the ORT8850 FPSC data sheet that is Exhibit 1005 in this proceeding—Mr. Britton testified on cross-examination that he was personally familiar with it, that he was "pretty sure I probably wrote most of it" and that he was "familiar with the Data Sheet. And I wrote most of that Data Sheet." *Id.* at 53:15–54:7. He further testified that he had "looked through it to believe that it looked like what I would have published at that time with that type of information." *Id.* at 56:14–16. On re-direct, regarding Lucent's standard practice of publishing information about its products on its website, Mr. Britton testified that he had "seen the webpages that was being reviewed that I - - I was signing off

on was the webpage. I definitely remember that at the time of the press release and the time of the Data Sheet." *Id.* at 71:17–72:7.

Exhibit C of the Britton declaration is an archived copy of Lucent's ORCA landing page captured on November 10, 2000. Ex. 1018 ¶ 10, Ex. C. It has a section entitled "New Documentation" with links next to four bullet points and a second section entitled "In the News" with a link next to a single bullet point. *Id.*, Ex. C. The link in the "New Documentation" section next to the second bullet point is entitled "ORT8850 FPSC Eight Channel x 850 Mbits/s Backplane Transceiver Data Sheet." *Id.* The Data Sheet attached as Exhibit E of the Britton declaration has the same title. *Id.*, Ex. E. The link next to the bullet point in the "In the News" section is entitled "Lucent Technologies Boosts Field-Programmable Gate Array (FPGA) Performance for Broadband Communications Applications Press Release." *Id.*, Ex. C. The press release attached to the Britton declaration as Exhibit B has the same title. *Id.*, Ex. B. On cross-examination, Mr. Britton testified that he was "definitely sure I clicked on that in the 2000s" in order "to see where the press release was and – and the Data Sheet was." Ex. 2011, 41:6–14, 42:20–43:6. Mr. Britton also testified that the link to the ORT8850 Data Sheet pointed to www.lucent.com/micro/netcom/docs/DS00406.pdf, and that DS00406 was "a document identifier following the naming convention we used at the time. DS was short for Data Sheet and 00406 identified a particular data sheet, in this case the one corresponding to the ORT8850 FPSC." Ex. 1018 ¶¶ 11–12.

Exhibit D of the Britton declaration is an archived copy of Lucent's FPSC product landing page captured on December 8, 2000. *Id.* ¶ 13, Ex. D. It lists a number of Lucent FPSCs, and for each, has a table that identifies the FPSC by "Part" number, includes a brief "Description," and where

applicable, provides links to "Application Note," "Data Sheet," "Manual," "Product Brief," and "Other" documents. *Id.*, Ex. D. The "Data Sheet" link for the ORT8850 FPSC is entitled "DS00406.pdf." *Id.* Mr. Britton testified that this link also pointed to www.lucent.com/micro/netcom/docs/DS00406.pdf, i.e., to "the same url provided by the webpage shown in Exhibit B [sic, C]." *Id.* ¶ 14.

Exhibit F of the Britton declaration is an archived copy of a Lucent webpage entitled "Index of /micro/netcom/docs/" captured on January 24, 2001. *Id.* ¶ 18, Ex. F. Mr. Britton testifies that it was the standard practice of the Lucent Netcom group to store documents such as datasheets, product briefs, and application notes in this web directory. *Id.* Exhibit F contains a list of document links identified by "Name," "Last modified," "Size," and "Description." *Id.*, Ex. F. Mr. Britton testifies that "consistent with our standard practices for publishing documents on the Lucent website," Exhibit F shows that the document pointed to by "the hyperlinks on the customer-facing webpages shown in Exhibits B and C [sic C and D]," i.e., www.lucent.com/micro/netcom/docs/DS00406.pdf, "was uploaded to the Lucent website on September 6, 2000 at 12:58 pm" as indicated in the "Last modified" column. *Id.* ¶ 19.

Mr. Britton further testifies that "the last page of Exhibit D [sic, E] identifies the document as 'DS00-406FPGA'" and that this indicates that Exhibit E "is the same document that was stored at the url identified in Exhibits C and D (www.lucent.com/micro/netcom/docs/DS00406.pdf)." *Id.* ¶ 16.

We find that the totality of the evidence, described above, is sufficient to authenticate Exhibit E of Mr. Britton's declaration under FRE 901(b)(3), because Mr. Britton is a witness with knowledge who has provided

sufficient testimony regarding its authenticity. We also find that the content of Exhibit E is not hearsay under FRE 803(6) because Mr. Britton is a qualified witness who has testified that it is a record of a regularly conducted business activity. We further find Exhibit E was published no later than September 6, 2000—the "Last modified" date for the document stored at www.lucent.com/micro/netcom/DS00406.pdf. Ex. 1018 ¶ 19, Ex. F. Alternatively, we find it was published no later than November 10, 2000, because that is the date the Internet Archived captured Exhibit C, which has a link to Exhibit E, and Mr. Britton testified that it was his regular practice to download all documents he was responsible for publishing and that he had clicked on that link in the 2000s to make sure the document was there. Ex. 2011, 41:6–14, 42:20–43:6, 47:16–48:7. We further find that Exhibit 1005 is authentic. its content is not hearsay, and it was published no later than September 6, 2000 or November 10, 2000 for the same reasons because Exhibit 1005 is a copy of Exhibit E of Mr. Britton's declaration.

We further note that Mr. Britton testifies that "[i]t was Lucent's regular practice at the time to publish preliminary data sheets on our website, as set forth above with respect to the September 2000 Data Sheets. By contrast, data sheets marked 'Advanced' were kept for internal use." Ex. 1023 ¶ 21. Mr. Britton's testimony, discussed above, shows that ORT8850 was a "preliminary" data sheet published on Lucent's customer-facing web pages and that customers expected this document to be available. *See Valve*, 8 F.4th at 1374 ("We have previously held that where a publication's purpose is 'dialogue with the intended audience,' that purpose indicates public accessibility."). Accordingly, for the reasons discussed above, we deny Patent Owner's motion to exclude Exhibit 1005 and Exhibit

E and paragraph 15 of the Britton declaration as hearsay or for lack of authentication.

3. QL80FC

Petitioner contends that QL80FC is an August 2000 data sheet from QuickLogic that was publicly accessible by September 3, 2000. Pet. 82 (citing Ex. 1008, 1). Petitioner submits the Affidavit of Elizabeth Rosenberg in support of its contention. *Id.* (citing Ex. 1019). Ms. Rosenberg testifies that she is a Records Request Processor at the Internet Archive, and that attached to her Affidavit as Exhibit A is a true and accurate copy of the archived webpage "for the URLs and the dates specified in the footer" of the Exhibit. Ex. 1019 ¶¶ 1, 6. That footer indicates Exhibit A is a copy of "http://www.quicklogic.com:80/devices/QuickFC/Default.htm" archived on September 3, 2000. *Id.* at 4. Petitioner argues Exhibit A indicates the "QuickFC Device Datasheet" was last updated in August 2000, and that is "consistent with the 'last updated' date of August 25, 2000 printed on the cover of the QL80FC datasheet." Pet. 82 (citing Ex. 1019, Ex. A; Ex. 1008, 1). Therefore, Petitioner argues, "QL80FC was published and publicly available on QuickLogic's website on at least September 3, 2000." *Id.*

Patent Owner argues we should exclude Exhibit 1008 for lack of authentication under FRE 901 and exclude Petitioner's reliance on the date printed on the face of that document as hearsay under FREs 801 and 802. Mot. 14. Patent Owner argues "the Rosenberg Affidavit neither references QL80FC nor makes any assertion of a connection between QL80FC and the webpages shown in the printouts" and, therefore, "does not authenticate Exhibit 1008 [QL80FC]." *Id.* Patent Owner further argues that the date printed on Exhibit A of the Rosenberg declaration indicating the last update

of the "QuickFC Device Datasheet" should be excluded as hearsay. *Id.* at 15.

Petitioner argues Exhibit 1008 "bears the name and label of QuickLogic on each page, and has the same appearance, contents, and substance consistent with technical datasheets made available to customers on manufacturer webpages at the time." Opp. 14. Therefore, Petitioner argues, Exhibit 1008 is authenticated under FREs 901(b)(4) and 902(7). *Id.* Petitioner further argues that because Dr. Nelson relied on Exhibit 1008 to show relevant data communication protocol features that were known to persons skilled in the art at the time, Exhibit 1008 should not be excluded pursuant to FRE 703.

Patent Owner argues that: (1) FRE 901(b)(4) cannot be used to demonstrate the public availability of a document, (2) FRE 902(7) only authenticates inscriptions, signs, tags, or labels, not the documents they may be attached to, and (3) "Petitioner cannot overcome the hearsay nature of Exhibit 1008 by having its expert rely upon that exhibit under Rule 703." Mot. Reply 5.

Upon considering all of the evidence and the arguments presented by the parties, we find Petitioner has failed to authenticate Exhibit 1008, and that the dates printed on the faces of Exhibit 1008 and Exhibit A of the Rosenberg declaration are hearsay. Exhibit A of the Rosenberg declaration contains two archived versions, dated September 3, 2000 and October 23, 2000, of the webpage www.quicklogic.com/devices/QuickFC/Default.html. Ex. 1019, Ex. A. The "second page" of the archived webpage contains a link entitled "QuickFC Device DataSheet." *Id.* However, as Patent Owner correctly argues, "the Rosenberg Affidavit only purports to 'attest[] to the authenticity of the archived and dated QuickFC ***webpages***'—not the

purportedly linked to [QL80FC] exhibits" and "[t]he Rosenberg Affidavit neither references QL80FC nor makes any assertion of a connection between QL80FC and the webpages shown in the printouts." PO Resp. 53–54. Petitioner offers no testimony from a custodian of records for the QL80FC product, as they did for the ORT8850 product, to support a finding that Exhibit 1008 is what Petitioner purports it to be. *See* Fed.R.Evid. 901(a).

Moreover, we disagree with Petitioner's contentions that FREs 703, 901(b)(4) or 902(7) authenticate or provide a basis to forego excluding Exhibit 1008. FRE 703 allows an expert to base his or her opinion on facts or data an expert in the field would reasonably rely on, even if they are not themselves admissible. *Id.* 703. They do not prohibit the exclusion of inadmissible evidence or allow for the admission of otherwise excludable evidence. Although FRE 901(b)(4) does allow evidence to be admitted based on its "appearance, contents, substance, internal patterns, or other distinctive characteristics," Petitioner has not shown that Exhibit 1008 contains sufficient distinctive characteristics to authenticate it. The only characteristic of Exhibit 1008 that tends to show that it is a QuickLogic datasheet for the QL80FC product is the appearance of QuickLogic's name and logo on the datasheet. *See* Ex, 1008. But Petitioner fails to present authenticated versions of other QuickLogic data sheets to demonstrate how the structure, format, and appearance of QL80FC is consistent with their structure, format, and appearance. *See* Pet. Reply 22–23; Opp. 14–15. Finally, FRE 902(7) does not authenticate Exhibit 1008, it only authenticates any "inscription[s], sign[s], tag[s], or label[s]" affixed to Exhibit 1008. *See* Fed.R.Evid. 902(7).

Accordingly, for the reasons discussed above, we find Petitioner has failed to authenticate Exhibit 1008, and we exclude Exhibit 1008 from this proceeding.

B. Level of Ordinary Skill in the Art

Petitioner identifies a person of skill in the art ("POSITA") at the time of the invention as someone that "would have had at least the equivalent of a Bachelor's degree in electrical engineering, computer engineering, or related field and 3-5 years of professional experience in computer systems design, circuit design, or equivalent academic experience." Pet. 5 (citing Ex. 1003 ¶¶ 4–6). We adopted this definition in our Institution Decision, sans the requirement that a skilled artisan have "at least" the level of education or experience indicated, as commensurate with the problems and solutions disclosed in the prior art of record. *See* Dec. Inst. 18–19 (citing *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995)). Patent Owner does not dispute that finding here, which we maintain in this Decision. *See* PO Resp. 6–7.

Patent Owner does argue that because Petitioner's declarant, Dr. Nelson, opined that a person with a master's degree and 3–5 years of experience in the fields described above would qualify as a person skilled in the art, his testimony and "opinions deserve little or no weight." *Id.* Petitioner responds that because Dr. Nelson confirmed in his Reply declaration that his "analysis necessarily included the low end of the spectrum of education and experience," it still holds true and should be accorded full weight. Pet. Reply 3–4.

We agree with Petitioner. Dr. Nelson's opinion that a person skilled in the art would have had *at least* the education and experience indicated necessarily encompasses persons having the minimum level of education and experience. It is axiomatic that something that was known or would

have been obvious to a person having a minimum level of education and experience would necessarily have been known or obvious to a person having the same or a higher level of education or experience. As we indicated in our Institution Decision, "the level of skill in the art is a prism or lens through which a judge, jury, or the Board views the prior art and the claimed invention." *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). In our analysis below, we consider all evidence as if viewed by a person having the minimum level of education and experience identified by Dr. Nelson, i.e., having "the equivalent of a Bachelor's degree in electrical engineering, computer engineering, or related field and 3-5 years of professional experience in computer systems design, circuit design, or equivalent academic experience." Ex. 1003 ¶ 6.

C. Claim Construction

Claims in an *inter partes* review are interpreted "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). Under that standard, the "words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp*., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citation omitted). Moreover, that meaning applies "unless the patentee demonstrated an intent to deviate from [it] . . . by redefining the term or by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Teleflex, Inc. v. Ficosa N. America Corp*., 299 F.3d 1313, 1327 (Fed. Cir. 2002); *see also Hill-Rom Servs., Inc. v. Stryker Corp*., 755 F.3d 1367, 1371 (Fed. Cir. 2014). Finally, only claim terms which are in controversy need to be construed and only to

the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner requests express constructions for the terms "programmable fabric" and "programmable fabric circuitry," and the parties dispute the scope of the plain and ordinary meaning of "a plurality of transceivers containing respective components having selectable values, said components being configured by said plurality of configuration memory cells, wherein one of said components is a loss of synchronization detector" (the "transceiver components" term). *See* Pet. 10; Pet. Reply 4–6; PO Resp. 8–11; PO Sur-Reply 4–6. We consider these terms below.

1. Programmable Fabric / Programmable Fabric Circuitry

Petitioner contends these terms "refer to user programmable circuitry capable of being programmed to implement arbitrary, as opposed to specific, logic functions." Pet. 10. In our Institution Decision, we determined the precise meanings of these terms were not in dispute and, therefore, declined to expressly construe them. *See* Dec. Inst. 19–20 (citing *Nidec Motor*, 868 F.3d at 1017). Neither party disputes that finding, which we maintain here. *See* PO Resp. 8; Pet. Reply 3–30.

2. Transceiver Components

This term is recited in claim 1 only. *See* Ex. 1001, 6:32–36. In our Institution Decision, we preliminarily determined that the plain and ordinary meaning of this term required an LOS detector that was "a transceiver component having selectable values that [was] configured by the plurality of configuration memory cells." Dec. Inst. 24.

Patent Owner agrees with this preliminary construction. *See* PO Resp. 9 ("The Board correctly found that [this term] requires a 'loss of synchronization detector' 'having selectable values,' 'being configured by

said plurality of configuration memory cells.'"). Patent Owner contends the term contains three interlocking clauses, where "[e]ach clause builds upon the former—requiring, when read together, the ordinary meaning previously understood by the Board." PO Sur-Reply 4. Patent Owner argues our preliminary construction is reinforced by the Specification, which "enumerat[es], in significant detail, 'configuration options' that provide the 'selectable values' for each and every component discussed, including the LOS detector." *Id.* (citing Ex. 1001, 3:43–54, 4:8–14, 4:56–58, 4:67–5:10, 5:13–22, 5:26–40, 5:51–60, 5:66–6:8).

Petitioner disagrees with our preliminary construction of this term, arguing that the claim language "simply requires transceivers containing a collection of components which have selectable values as a collective entity . . . [and] does not require each of these components to be configurable and to have selectable values." Pet. Reply 4–5 (emphasis omitted). Petitioner further argues "claim 1 does not say that 'each' component is configurable, or that 'each' has selectable values" and "does not refer to the LoS detector as a 'configurable LoS detector.'" *Id.* at 5. Petitioner also argues that because claim 1 expressly requires other transceiver components to be configurable (e.g., the serializer), our preliminary interpretation would render the term "configurable" superfluous with respect to those components. *Id.* at 6 (citing *Power Mosfet Techs., L.L.C. v. Siemens AG,* 378 F.3d 1396, 1410 (Fed. Cir. 2004)).

Upon consideration of the arguments and evidence presented, we maintain our preliminary construction that the plain and ordinary meaning of the transceiver component limitation requires the LOS detector to be "a transceiver component having selectable values that is configured by the plurality of configuration memory cells." The limitation requires "a

plurality of transceivers containing respective components having selectable values," wherein "*said* components [are] configured by . . . memory cells," and wherein "one of *said* components is a loss of synchronization detector." Ex. 1001, 6:32–36 (emphases added). Thus, the LOS detector is one of the transceiver components referred to earlier, i.e., one of "said components" "having selectable values" that is "configured by . . . memory cells." *Id.* The Specification is consistent with this interpretation. It discloses a transceiver whose receiver side includes deserializer/comma detector 174, decoder 178, elastic buffer 182, CRC 186, and LOS 188.[10] *Id.*, Fig. 3. Each of these components is described as being configurable and having selectable values. *Id.* at 4:54–6:7.

Moreover, our interpretation does not render superfluous the use of the term "configurable" in other limitations. To the contrary, the transceiver components limitation only requires transceiver components identified as "one of said components," i.e., as one of the "respective components having selectable values" to be configurable. It does not require every transceiver component to be configurable because not every transceiver component has to be identified as "one of said components." Thus, because the serializer and deserializer are not identified as "one of said components" in the "transceiver components" limitation, that limitation does not require that they be configurable. As a result, the claim's later requirement of "a configurable serializer" and "a configurable deserializer" is not superfluous.

[10] We only consider the receiver side of the transceiver, because only the receiver side has a loss of synchronization detector.

D. Challenges Based on OneChip and ORT8850

Petitioner argues claims 1–5, 8–12, and 15–17 are unpatentable as obvious over OneChip and ORT8850. Pet. 19–60; Pet. Reply 4–20. Patent Owner disagrees. PO Resp. 8–32; PO Sur-Reply 3–22. For the reasons discussed below, notwithstanding Patent Owner's arguments to the contrary, we find Petitioner has demonstrated by a preponderance of evidence that claims 1–5, 8–12, and 15–17 are unpatentable over OneChip and ORT8850.

1. OneChip

OneChip discloses a processor architecture that "combines a fixed-logic processor core with reconfigurable logic resources." Ex. 1004, 126. This architecture is illustrated in Figure 6 of OneChip, a Petitioner-colorized version of which is reproduced below.

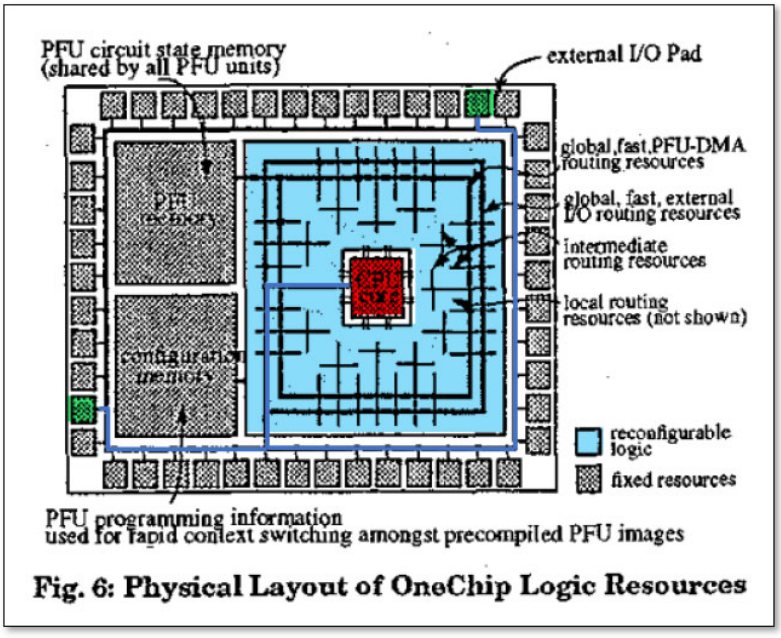


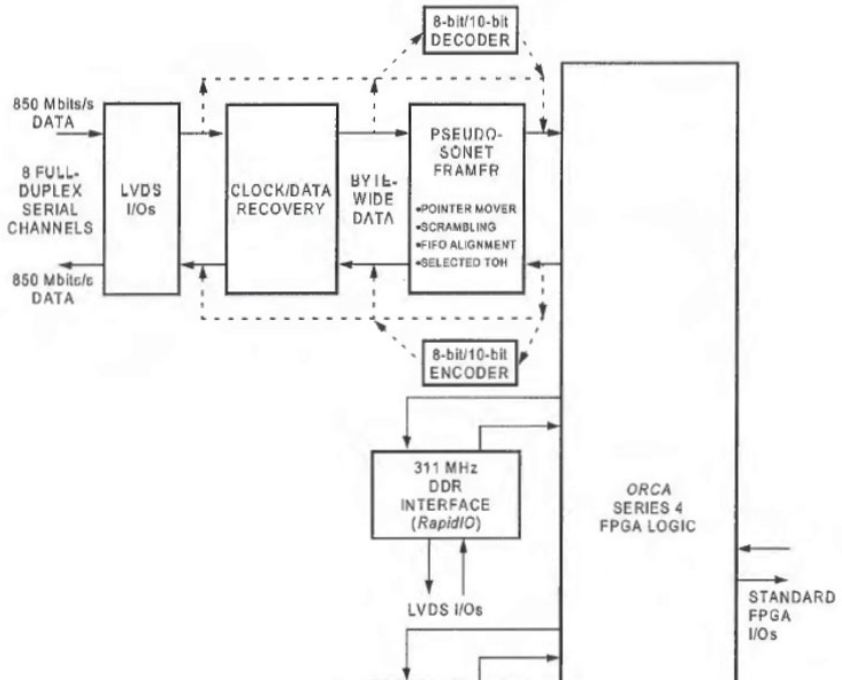
Fig. 6: Physical Layout of OneChip Logic Resources

The figure above is a Petitioner-colorized version of Figure 6 of OneChip. Pet. 20. The figure shows the physical layout of OneChip's logical resources, including a CPU (red) surrounded by reconfigurable logic (blue) and having configuration memory (bottom, left), all surrounded by

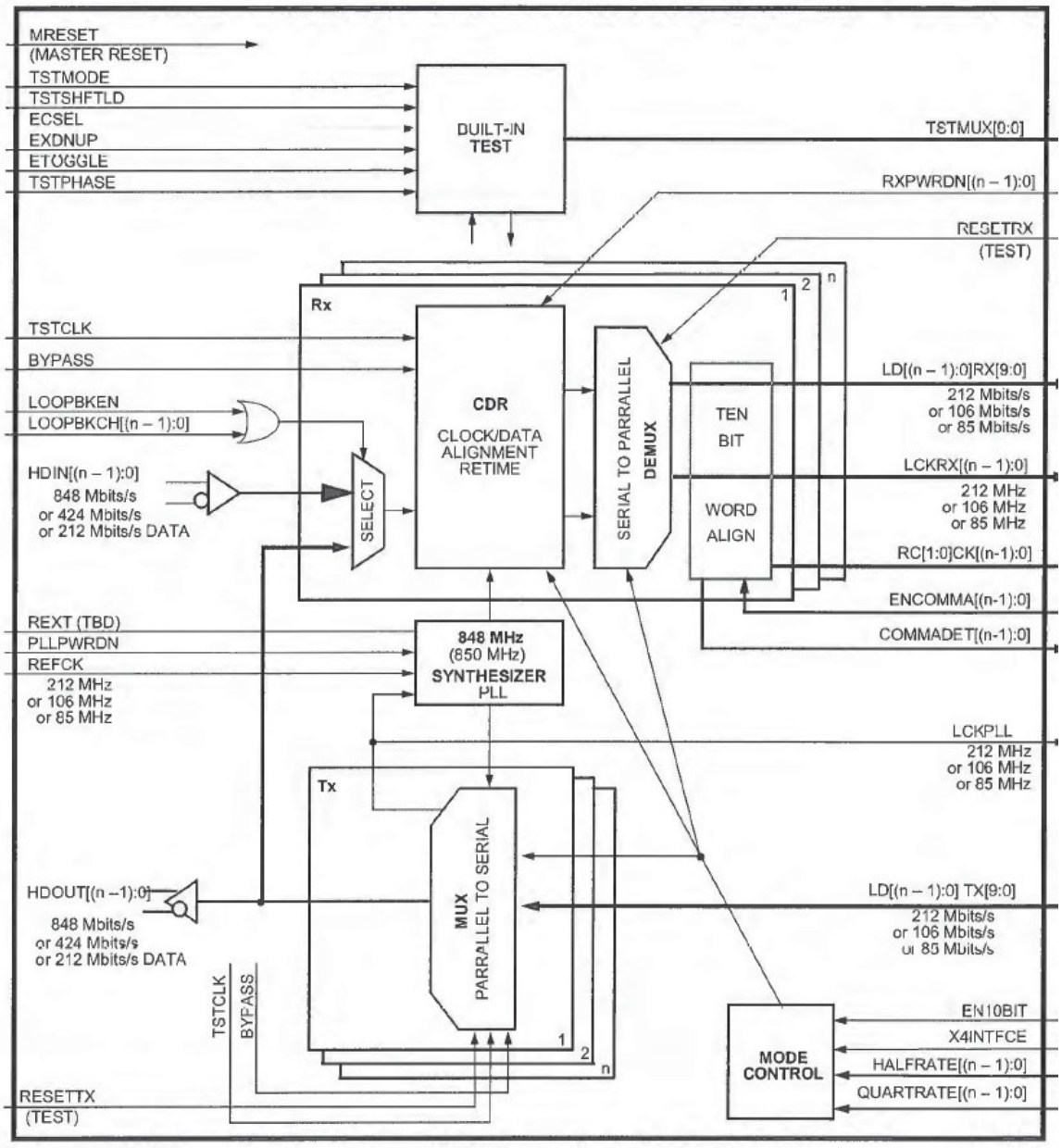
peripheral I/O (input/output). Ex. 1004, 130. The reconfigurable logic includes "programmable function units (PFU[s])" that can "implement many application specific functions" and "can also be used as programmable glue logic." *Id.* at 129.

2. ORT8850

ORT8850 is a preliminary data sheet for the ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver. Ex. 1005, 1. The ORT8850 chip is "a high-speed backplane transceiver combined with FPGA logic" that facilitates "high-speed serial transfer of data in a variety of applications including Gigabit Ethernet [and] fibre channel" and provides "8B/10B coding/decoding for each channel." *Id.* at 12, 15. A portion of a block diagram of the ORT8850 FPSC is illustrated in Figure 1, which is reproduced below. *Id.* at 13.



The figure is a portion of a block diagram of the ORT8850 FPSC. *Id.* It includes an LVDS (low voltage differential signaling) input/output (I/O), and a high speed interconnect (HSI) interface to ORCA series 4 FPGA logic. *Id.* A block diagram of the HSI is shown in Figure 3, which is reproduced below. *Id.* at 18–19.



The figure above is Figure 3 of ORT8850, which is an HSI Functional Block Diagram. *Id.* at 19, Fig. 3. For each of n channels, the HSI interface

receives LVDS serial data (HDIN) at one of three data rates (848, 424, or 212 Mbits/s), converts the data to byte-wide data (LD) using a Serial-to-Parallel Demux, and transmits the byte-wide data to the FPGA logic. *Id.* at 15, 19. Similarly, for each of n channels, the HSI interface receives byte-wide data (LD) from the FPGA logic, converts it to serial data (HDOUT) using a Parallel-to-Serial Mux, and transmits the serial data to the LVDS I/O. *Id.* Control signals EN10BIT, HALFRATE, and QUARTRATE provided to both the Serial-to-Parallel Demux and Parallel-to-Serial Mux allow these devices to receive/transmit full-rate (848 Mbits/s), half-rate (424 Mbits/s), or quarter-rate (212 Mbits/s) data, and to optionally encode/decode the data using 8B/10B encoding. *Id.*

3. Reasons to Combine OneChip and ORT8850

Relying on the testimony of Dr. Nelson, Petitioner argues industry trends, including the trend to combine processor cores with configurable, multi-protocol transceivers on programmable devices, would have suggested the combination of OneChip and ORT8850. *See* Pet. 24–25 (citing Ex. 1003 ¶ 42). Further relying on the testimony of Dr. Nelson, Petitioner argues that, because OneChip teaches "a processor core surrounded by a programmable fabric and embedded I/O circuitry," a person of ordinary skill in the art would have known "the configurable transceivers described in ORT8850 . . . could be easily implemented in OneChip" and would have been motivated to make the combination to improve "OneChip's I/O circuitry by providing a flexible, high-speed data communication interface to external devices." *Id.* at 25–27 (citing Ex. 1003 ¶¶ 42–44).

Notwithstanding Patent Owner's arguments to the contrary, discussed *infra*, we find Petitioner has articulated persuasive reasoning with rational underpinning to combine the teachings of OneChip and ORT8850. First, we

credit Dr. Nelson's unrebutted testimony that industry trends supported the combination. Ex. 1003 ¶¶ 27–31, 42–46. Second, we agree with Dr. Nelson that OneChip and ORT8850 motivated the combination because OneChip discloses "a processor core surrounded by a programmable fabric and embedded I/O circuitry" and "using the known technique of ORT8850's configurable transceivers would have improved OneChip's I/O circuitry by providing a flexible, higher-speed data communication interface." *Id.* ¶¶ 42, 44. "[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR Int'l v. Teleflex Inc.,* 550 U.S. 398, 417 (2007) (internal citation omitted).

Patent Owner provides several arguments against the combination of OneChip and ORT8850. First, Patent Owner argues that, because OneChip's Table 1 shows that "OneChip used parallel I/O ports to transmit and receive data in bytes" and ORT8850 used "serial I/O ports," a person of ordinary skill in the art would not have "replace[d] OneChip's parallel I/O ports . . . with ORT8850's SERDES and serial I/O ports." PO Resp. 19–21 (citing Ex. 1004, 132; Ex. 2013 ¶¶ 44–50). Petitioner replies that Table 1 "also lists 'UART' (*i.e.*, universal asynchronous receiver-transmitter) as one of OneChip's possible applications" and "UART is a serial interface." Pet. Reply 15 (citing Ex. 1004, 132; Ex. 1030 ¶¶ 20–21). Patent Owner counters that Petitioner's proposed combination is to replace OneChip's "parallel 'external I/O pads'" with ORT8850's transceivers and OneChip's UART is internal circuitry that is distinct from its I/O pads. PO Sur-Reply 19.

We disagree with Patent Owner's contentions. First, Petitioner's proposed combination is not to replace OneChip's I/O pads with ORT8850's

transceivers, but to modify OneChip so that "[t]he result would be OneChip's single-chip design having a processor core surrounded by a programmable fabric with I/O circuits at the periphery." Pet. 24. Second, Table 1 of OneChip illustrates programming OneChip to emulate a UART, which is "a serial interface used for decades for long haul communications." Ex. 1004, 132; Ex. 1030 ¶ 21. Thus, it would have been obvious to replace OneChip's programmed UART I/O circuitry with ORT8850's configurable SERDES I/O circuitry.

Patent Owner next argues that a person skilled in the art would not have used OneChip's memory to configure ORT8850's transceivers because "[t]he sole purpose of OneChip's configuration memory is to configure FPGA modules." PO Resp. 23. Petitioner replies that OneChip's memory "is agnostic to the device that the memory will communicate with" and the fact that it "is used to control FPGA-based blocks does not prevent [it] from being able to interface and communicate with . . . ORT8850s transceivers." Pet. Reply 16 (citing Ex. 1030 ¶ 24). We agree with Petitioner. Although there are different types of computer memory, nothing in OneChip suggests its memory can only configure FPGAs and nothing in ORT8850 suggests its transceivers require any type of specialized configuration memory.

Finally, Patent Owner also argues that a person skilled in the art would not have been able to combine the teachings of OneChip and ORT8850 with a reasonable expectation of success. *See* PO Resp. 25–27. First, Patent Owner argues such a person "would have had no chance of success in using OneChip's configuration memory . . . to configure ORT8850's SERDES." *Id.* at 26. We disagree for the reasons discussed above. Next, Patent Owner argues OneChip was "an aspirational system" that was not enabled because it (a) was "prototyped using an entirely

different architecture" that only "emulate[d] the OneChip configuration" and had not been "implemented in custom silicon," and (b) left unresolved the relative proportions of control, datapath, and RAM logic, and required certain "non-trivial" steps to be developed before "a user-friendly OneChip processor will be found in the heart of future commercial products." *Id.* at 12–16 (quoting Ex. 1004, 130, 134–135; Ex. 2013 ¶¶ 28–37) (emphasis omitted). Therefore, Patent Owner argues, because OneChip was not enabled its combination with ORT8850 was also not enabled and could not be made with reasonable expectation of success. *Id.* at 12–13, 26 (citing *Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1376–77 (Fed. Cir. 2021).

We disagree with Patent Owner's contentions. First, OneChip is presumed to be enabled and Patent Owner bears the burden to prove otherwise. *See Apple Inc. v. Corephotonics, Ltd*., 861 Fed. Appx. 443, 450 (Fed. Cir. 2021) ("[R]egardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement."). Patent Owner does not prove OneChip was not enabled because its design was only emulated, it was not built in custom silicon, it did not specify relative amounts of various components, or it had not worked out all of the issues needed for a commercial product. *See In re Donohue*, 766 F.2d 531, 533 (Fed. Cir. 1985) ("It is not, however, necessary that an invention disclosed in a publication shall have actually been made in order to satisfy the enablement requirement."); *see also CFMT, Inc. v. Yieldup Int'l Corp.*, 349 F.3d 1333, 1338 (Fed. Cir. 2003) ("Enablement does not require an inventor to meet lofty standards for success in the commercial marketplace.").

Second, even if OneChip was not enabled, its teachings nonetheless "qualify as prior art for the purpose of determining obviousness under § 103." *Symbol Techs., Inc. v. Opticon, Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991). OneChip teaches integrating a processor, programmable logic, memory, and peripheral I/O resources on a single chip. Ex. 1004, 126, 130, Figs. 1, 6. ORT8850 teaches integrating programmable logic, memory, and programmable transceivers on a single chip. Ex. 1005, 12, 15. "To render a claim obvious, *the prior art, taken as a whole, must enable* a skilled artisan to make and use *the claimed invention*." *Raytheon*, 993 F.3d at 1380 (emphasis added); *see also In re Kumar*, 418 F.3d 1361, 1369 (Fed. Cir. 2005) ("To render a later invention unpatentable for obviousness, *the prior art must enable . . . the later invention*.") (emphasis added). Thus, the relevant inquiry is not whether OneChip was enabled when it was published, but whether a person skilled in the art would have been able to combine the relied-upon elements of OneChip and ORT8850 at the time of the invention claimed in the '709 patent.

The '709 patent describes and claims an integrated circuit containing a processor core, programmable fabric, plurality of configurable transceivers, and memory to configure the transceivers and programmable fabric. Ex. 1001, 1:35–46, 7:1–23, Fig. 1. However, the '709 patent does not disclose *how* to integrate these components on a single chip or suggest that doing so would be beyond the level of skill of a person of ordinary skill in the art. *Id.* at 1:64–2:25. But the '709 patent is presumptively enabled. *See* 35 U.S.C. § 282(a). Therefore, a person of ordinary skill in the art at the time of the invention would have known how to successfully integrate a processor, programmable logic, configuration memory, and I/O resources on a single chip, as taught by both the '709 patent and OneChip. *See In re*

Epstein, 32 F.3d 1559, 1568 (Fed. Cir. 1994) ("[T]he Board's observation that appellant did not provide the type of detail in his specification that he now argues is necessary in prior art references supports the Board's finding that one skilled in the art would have known how to implement the features of the references . . . ."). OneChip's enablement at least by the time the '709 patent was filed distinguishes over *Raytheon*, where the prior art was not enabled because the "advanced material" it disclosed was unavailable not only when the prior art was published, but when the challenged patent was filed. *See Raytheon*, 993 F.3d at 1379, 1382 (finding patent owner had presented unrebutted evidence the "advanced material" disclosed in the prior art was unavailable and its exceptional properties "had not been achieved through other means as of the priority date" of the challenged patent, and patent challenger "did not dispute that [the prior art's] contemplated revolutionary materials were unavailable at the time the [challenged] patent was filed").

4. Claim 1

Claim 1 recites an IC comprising a plurality of configuration memory cells coupled to a programmable fabric such that the memory cells can be programmed to implement a circuit in the programmable fabric. Ex. 1001, 6:25–31. Petitioner demonstrates how OneChip teaches these limitations, and persuasively illustrates its contentions with a colorized version of Figure 6 of OneChip, which is reproduced below. *See* Pet. 28–32 (citing Ex. 1004, 126, 129, 130, Figs. 1, 6).

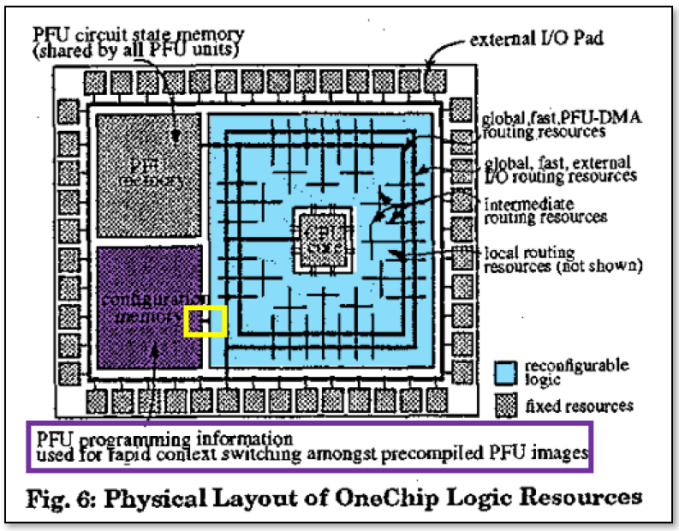


Fig. 6: Physical Layout of OneChip Logic Resources

The figure above is a Petitioner-colorized version of Figure 6 of OneChip. *See* Pet. 31. It shows a CPU core surrounded by "reconfigurable logic" (blue) that is configurable by "configuration memory" (purple). The reconfigurable logic is in the form of "programmable functional units" (PFUs) that can "implement many application specific functions" and "any combinational or sequential circuit." Ex. 1004, 129. The "configuration memory" can store "pre-compiled PFU images" in order to implement these functions. *Id.* at 130. Patent Owner does not dispute this. *See* PO Resp. 8–31.

Claim 1 further requires the IC to include "a plurality of transceivers containing respective components having selectable values, said components being configured by said plurality of configuration memory cells, wherein one of said components is a loss of synchronization detector." Ex. 1001, 6:32–36. As discussed in § II.C.2, *supra*, we construe this term to require each of the plurality of transceivers to have a loss of synchronization detector "having selectable values that is configured by the plurality of configuration memory cells."

Petitioner relies on ORT8850 to teach this limitation. *See* Pet. 32–36; Pet. Reply 6–9. Petitioner argues ORT8850 teaches a plurality of transceivers, each having components having selectable values that are configured by memory, such as SERDES components that can be configured to operate at selectable data rates. *See* Pet. 33–34 (citing Ex. 1005, 19, Fig. 3). Petitioner further argues a person of ordinary skill in the art would have known that ORT8850's transceivers include a LOS detector because they can detect data streams formatted according to both Fibre Chanel and SONET protocols. *Id.* at 35–36 (citing Ex. 1003 ¶¶ 57–58). Specifically, Petitioner argues, ORT8850's transceivers can detect "invalid characters, or special command characters, or loss of signal" in Fibre Channel data streams and "special framing pattern characters known as 'A1' and 'A2' or loss of signal" in SONET data streams. *Id.*

In our Institution Decision, we questioned whether Petitioner would be able to demonstrate that ORT8850's transceivers have a configurable LOS detector as required by claim 1. *See* Dec. Inst. 25. Patent Owner argues Petitioner cannot because Petitioner "never pointed to a LOS detector in ORT8850" and "[n]othing in the Petition establishes a LOS detector with selectable values." PO Resp. 10.

Petitioner replies that, even if this limitation requires a configurable LOS detector having selectable values, ORT8850 meets it because ORT8850 "is expressly intended to support multiple communication protocols, including Fibre Channel and SONET" and a person of ordinary skill in the art "would appreciate that LoS detection and the LoS detector would be enabled separately and configured differently for each standard." Pet. Reply 6–7 (citing Pet. 22, 35–36). Relying on the testimony of Dr. Nelson, Petitioner argues that when receiving SONET data, ORT8850's

"LoS function is performed 'by searching for special framing pattern characters known as 'A1' and 'A2' or loss of signal," and when receiving Fibre Channel data, by "monitor[ing] the data stream for invalid characters, special command characters, or loss of signal." *Id.* at 7, 9 (quoting Pet. 35–36; Ex. 1003 ¶¶ 57, 58).

Petitioner argues ORT8850's "framer block" performs the LOS function when receiving SONET data streams and can be selectively enabled/disabled by a bit in ORT8850's Memory Map table. *Id.* at 7–8 (citing Ex. 1005, 24–25, 45, 50; Ex. 1030 ¶¶ 8–11). Relying on the testimony of Dr. Nelson, Petitioner argues a person skilled in the art would have known that ORT8850's "LoS functions and components for each protocol [i.e., Fibre Channel and SONET] would be, at minimum, enabled or disabled . . . in a similar way as . . . the framer block." *Id.* at 9 (citing Ex. 1030 ¶¶ 12–13).

Patent Owner argues Petitioner's Reply includes a new theory that "should be disregarded as improper gap-filling." PO Sur-Reply 14. For example, Patent Owner argues "Petitioner did not identify any specific component in the ORT8850 as purportedly disclosing a 'loss of synchronization detector,'" but instead relied on Dr. Nelson's opinion that "the functionality would be obvious to include because it would be present in Fibre Channel and SONET protocols." *Id.* (citing Pet. 35–36). Patent Owner argues the enable/disable bit Petitioner identified in ORT8850's Memory Map table selectively enables the entire "Pseudo-SONET framer" shown in Figure 1, not the "framer block" component Petitioner identified as the LOS detector. *Id*. at 7–9. Patent Owner further argues Petitioner has failed to demonstrate ORT8850's "framer block" is a LOS detector because ORT8850 executes a "Pseudo-SONET" protocol rather than a SONET

protocol. *Id.* at 11. Patent Owner also argues that the "framer block" is not configurable because it describes "a fixed protocol of entering into an OOF [out-of-frame] state after two missed transitions." *Id.* at 10. Finally, Patent Owner argues Petitioner's "theory that Fibre Channel would have 'corresponding LoS functions and components' that could be enabled or disabled individually is . . . improper new argument" and "relies entirely on the mistaken new arguments, rebutted above, concerning SONET." *Id.* at 13.

Upon consideration of all the argument and evidence provided by Petitioner and Patent Owner, we find ORT8850's transceivers include a LOS detector having selectable values (e.g., enable/disable) that is configurable. ORT8850's transceivers can process either SONET or Fibre Channel data received over eight individual data channels. Ex. 1005, 15. When SONET data is received, a "framer block" "detects the A1/A2 framing pattern and generates the 8 kHz frame pulse" for each channel. *Id*. at 12, 24. The framer also detects loss of synchronization for each channel because it "increments an A1/A2 frame error counter" upon detecting an errored frame, and "after two transitions are missed [it] goes into the OOF state." *Id.*

When ORT8850 receives Fibre Channel data, it does 8B/10B decoding and "[f]rame synchronization and multi channel alignment . . . through the use of special K characters." *Id.* at 12; *see also* Ex. 1022, 18 (disclosing Fibre Channel "transmits information using an adaptive 8B/10B code"), 73 n.1 (disclosing Fibre Channel uses "the K28.1, K28.5 and K28.7 Special Characters [as] a singular bit pattern" that "is sufficient to identify the word alignment of the received bit stream"). ORT8850 also performs loss of synchronization detection in Fibre Channel mode because the protocol *requires* it. *See* Ex. 1022, 73 (a receiver "*shall* check each received

Transmission Word" and "*shall* remain in the Synchronization-Acquired state until the loss-of-Synchronization procedure . . . is completed"), 74 (disclosing five loss-of-Synchronization procedure detection states and that "[a] receiver in the fifth detection state . . . *shall* enter the Loss-of-Synchronization state") (emphases added).

Regardless of whether ORT8850 receives SONET or Fibre Channel data, its loss of synchronization detectors have selectable values that allow them to be enabled or disabled. For example, in SONET mode, an ORT8850 transceiver stores an 8-bit control word for each of its eight input channels in respective memory locations. This is shown in Table 10 of ORT8850, a modified portion of which is reproduced below. *See* Ex. 1005, 45.

ADDR [7:0]	Register Type	Register Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Reset Value (hex)	Comments
37, 4f, 67, 7f, 97, af, c7, df	creg	—	—	—	Framer Disable	Sync Control		LVDS redundant select	Bypass Alignment FIFO + Pointer Mover	Bypass Alignment FIFO only	0x00	—

The figure above is a version of ORT8850's memory location map (Table 10) modified to show only the 8-bit control word (DB0–DB7) stored at the eight memory locations (hexadecimal addresses 37, 4f, 67, 7f, 97, af, c7, df) corresponding to ORT8850's eight input channels. *Id.* at 36 (disclosing register type "creg" is a control register or "read and writable memory element inside core control"), 37 (disclosing "[a] full memory map is included in Table 10, followed by detailed descriptions in Table 11," and indicating each input channel has an address block with "the same structure" but with "a constant address offset between channel register blocks"). A modified portion of Table 11 of ORT8850 is reproduced below. *Id.* at 50.

Table 11. Memory Map Descriptions (continued)

Bit/Register Name(S)	Bit/Register Location (Hex)	Register Type	Reset Value (Hex)	Description
Bypass register	37,4f,67,7f,97,af ,c7,df[0]	creg	0x0	1 - Bypass Pointer Mover
Bypass register	37,4f,67,7f,97,af ,c7,df[1]	creg	0x0	1 - Bypass only Alignment fifo + Pointer Mover
Enable work/protect channels	37,4f,67,7f,97,af ,c7,df[2]	creg	0x0	Bit to control the LVDS drivers/receivers to/from CDR 0 - Use LVDS drivers and receivers to/from Pi-sched I/F block B (Work channels) 1 - Use LVDS drivers and receivers to/from Pi-sched I/F block C (Protect channels)
Sync Control register	37,4f,67,7f,97,af ,c7,df[4:3]	creg	2'b00	00 - No alignment 01 - Align with twin (i.e STM B stream A) 10 - Align with all 4 (i.e. STM A all streams) 11 - Align with all 8 (i.e. STM A and B all streams)
Disable Framer	37,4f,67,7f,97,af ,c7,df[5]	creg	0x0	0 - Enable framer 1 - Disable STS-12 framing

The figure above is a version of Table 11 of ORT8850, describing the contents of its memory map, modified to show only the contents of the 8-bit control word stored in the eight memory locations (hexadecimal addresses 37, 4f, 67, 7f, 97, af, c7, df) corresponding to its eight input channels. As shown in conjunction with Table 10, DB0 (data bit 0) controls whether a SONET stream bypasses a pointer mover block, DB1 controls whether the stream bypasses an alignment FIFO (first-in/first-out) buffer together with the pointer mover block, DB2 controls selection of an LVDS driver to drive the received SONET data stream, DB3 and DB4 control whether and how the stream is aligned with other SONET data streams received on other channels, and DB5 controls whether the SONET framer is enabled or disabled. *Id.* at 45, 50.[11]

The '709 patent discloses one way a LOS detector can be configured is by "us[ing] or bypass[ing] this detector." Ex. 1001, 5:66–6:1. Thus,

[11] As ORT8850 explains, the eight SONET channels are labeled AA–AD and BA–BD. Ex. 1005, 17, 25. DB3 and DB4 values determine whether a given channel is unaligned with other channels (00) or aligned with one (01), three (10), or seven (11) other channels via an alignment FIFO. *Id.* at 45, 50; *see also id.* at 25, Figs. 5–8 (illustrating various data stream alignments).

because ORT8850's "framer block" can be selectively enabled or disabled (used or bypassed) by bits stored in memory, it is a transceiver component having selectable values that can be configured by memory as required by claim 1. Moreover, we agree with Dr. Nelson's testimony that given ORT8850's teachings regarding the SONET "framer block," a person skilled in the art would have "expect[ed] that Fibre Channel would have analogous enable/disable 'selectable values,' as Fibre Channel itself is one of the many protocols expressly supported by ORT8850." Ex. 1030 ¶ 12 (cited in Pet. Reply 9).[12]

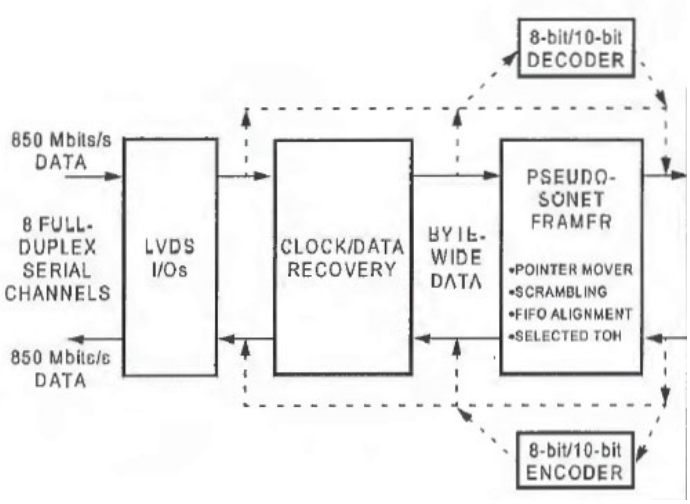
We disagree with Patent Owner's contention that we should disregard the arguments presented in Petitioner's Reply and Dr. Nelson's Reply Declaration for presenting "new" argument. *See* PO Sur-Reply 14–16. The Petition relies on ORT8850's support of both the Fibre Channel and SONET protocols and explains how these protocols identify special characters, unique to each, for LOS detection. *See* Pet. 35–36; Ex. 1003 ¶ 57. Petitioner, in its Reply, responds to our preliminary construction requiring a configurable LOS detector by explaining how ORT8850's "framer block," which is the component that detects SONET's A1 and A2 framing characters, determines loss of synchronization and can be selectively enabled/disabled based on values stored in memory. *See* Pet. Reply 7–8 (citing Ex. 1030 ¶¶ 8–11). Petitioner further responds by explaining why a person of ordinary skill in the art would have expected ORT8850 to use a configurable LOS detector (i.e., one that can be selectively enabled/disabled) to receive Fibre Channel data. *Id.* at 9 (citing Ex. 1030 ¶¶ 12–13). Thus,

[12] We note that ORT8850 expressly states that its "use of the 8B/10B [Fibre Channel] sync block is similar to that of the [SONET] block." Ex. 1005, 17.

Petitioner's Reply does not amount to new argument but to an explanation of why a person skilled in the art would have known not only that ORT8850 included LOS detectors for receiving SONET and Fibre Channel data as indicated in the Petition (*see* Pet. 35–36 (citing Ex. 1003 ¶¶ 57–58)), but that those LOS detectors would have been configurable because they would have needed to detect different special characters for SONET and Fibre Channel data (*see* Pet. Reply 7–9 (citing Ex. 1030 ¶¶ 8–13)).

Our rules allow Petitioner to "respond to arguments raised in the corresponding opposition, patent owner preliminary response, or patent owner response." 37 C.F.R. § 42.23(b). We also allow Petitioner "in its reply brief, to address issues discussed in the institution decision" and to "submit rebuttal evidence in support of its reply." CTPG 73. As the Federal Circuit has stated, "[t]he purpose of the trial in an inter partes review proceeding is to give the parties an opportunity to build a record introducing evidence—not simply to weigh evidence of which the Board is already aware." *Genzyme Therapeutic Prods. Ltd. P'ship v. Biomarin Pharm. Inc*., 825 F.3d 1360, 1367 (Fed. Cir. 2016).

We also disagree with Patent Owner's argument that the memory table bit Petitioner identified for selectively enabling/disabling the "framer block" instead "control[s] the two modes [Pseudo-SONET and 8B/10B] in which ORT8850 operates." PO Sur-Reply 8–9. Patent Owner's argument is based, in part, on its interpretation of Figure 1 of ORT8850, a portion of which is reproduced below.



Ex. 1005, 12. The Figure is a portion of a block diagram of the ORT8850 chip showing how ORT8850 receives/transmits data on 8 full-duplex serial data channels, deserializes/serializes the data, and decodes/encodes the data using either the SONET ("Pseudo-SONET") or Fibre Channel (8B/10B) protocol. As shown, the Pseudo-SONET framer performs a number of functions, including "pointer mover," "scrambling," "FIFO alignment," and "selected TOH." *Id.* It also performs other functions not shown in Figure 1, such as "framer block," "sampler," "AIS-L insertion," and "internal parity generation." *Id.* at 24–31. The "framer disable" bit Petitioner identified for selectively enabling/disabling the "framer block" is one bit (DB5) in an 8-bit control word that also controls whether a data stream should (a) bypass the "pointer mover" (DB0), (b) bypass both the "pointer mover" and "FIFO alignment" (DB1), (c) select particular LVDS receivers/drivers (DB2), and (d) align with other data streams in the alignment FIFO (DB3/4). *Id.* at 45, 50. Thus, DB5 of the control word does not enable/disable the "Pseudo-SONET framer" as a whole, as Patent Owner contends, but the "framer block" within the "Pseudo-SONET framer," just as the other bits in the control word enable/disable other components (e.g., pointer mover, FIFO alignment, and LVDS selection).

Claim 1 further requires each of the plurality of transceivers to include a configurable serializer/deserializer coupled to a configuration memory cell and configurable to transmit/receive data at a selected bit rate. Ex. 1001, 6:37–42. Petitioner demonstrates how ORT8850 teaches this limitation. *See* Pet. 36–41 (citing Ex. 1005, 12, 18–20, 24, Fig. 3; Ex. 1003 ¶¶ 59–65). ORT8850 discloses receiving "differential 850 MBits/s (or subrates 424 MBits/s, 212 MBits/s) serial data without clock at its LVDS receiver input." Ex. 1005, 18. Figure 3 of ORT8850 discloses a high speed interface (transceiver) that includes a serial-to-parallel demux (deserializer) and a parallel-to serial-mux (serializer), both of which can be programmed via a HALFRATE or QUARTRATE "Mode Control" signal. *Id.* at 19, Fig. 3. The deserializer can receive data at programmable rates of 848, 424, or 212 MBits/s and the serializer can transmit serial data at the same programmable rates. *Id.* Patent Owner does not dispute this. *See* PO Resp. 8–31.

Claim 1 further requires each of the plurality of transceivers to include input/output ports that receive/transmit differential input/output signals. Ex. 1001, 6:43–45. Petitioner demonstrates how ORT8850 teaches this limitation. *See* Pet. 41–43 (citing Ex. 1005, 18–19, Figs. 1, 3; Ex. 1003 ¶¶ 66–68). As discussed above, ORT8850 discloses receiving "differential 850 MBits/s (or subrates 424 MBits/s, 212 MBits/s) serial data without clock at its LVDS receiver input." Ex. 1005, 18. ORT8850 similarly discloses transmitting an "850 MBits/s serial data stream . . . through [its] LVDS driver." As noted in § II.D.2, *supra*, LVDS stands for low voltage *differential* signaling, and ORT8850 discloses its "LVDS drivers and receivers operate on a 100 Ω differential impedance" and its "differential driver and receiver buffers include termination resistors." *Id.* at 58. Patent Owner does not dispute this. *See* PO Resp. 8–31.

Claim 1 further requires a plurality of signal paths coupling each configurable transceiver to a circuit implemented in the programmable fabric and having at least a portion that passes through the programmable fabric. Ex. 1001, 6:46–50. Petitioner contends the combination of OneChip and ORT8850 teaches this limitation. *See* Pet. 43–45 (citing Ex. 1004, 129–130, Fig. 6; Ex. 1003 ¶¶ 69–73). Petitioner demonstrates its contentions with a colorized version of Figure 6 of OneChip, which is reproduced below.

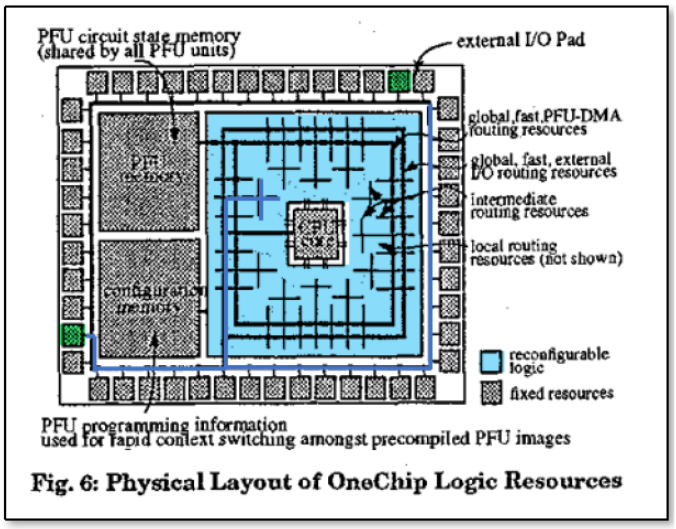


Fig. 6: Physical Layout of OneChip Logic Resources

The figure above is a Petitioner-colorized version of Figure 6 of OneChip. *See* Pet. 44. Petitioner contends that "OneChip's external I/O pads (green) are coupled to the reconfigurable logic (i.e., '*programmable fabric*') (blue) by routing resources (i.e., '*signal paths*') (dark blue)." *Id.* at 43–44 (citing/quoting Ex. 1004, 130). Petitioner argues that its colorized figure illustrates "two external I/O pads and their respective signal paths connected to the circuitry implemented in the programmable fabric" and that in the OneChip and ORT8850 combination, OneChip's routing resources "will run from the external I/O locations where ORT8850's transceivers are located to the circuitry of the reconfigurable logic." *Id.* at 45 (citing Ex. 1003 ¶ 73). We agree with Petitioner's contentions for the reasons stated in the Petition and

Petitioner's Reply. Patent Owner does not dispute them. *See* PO Resp. 8–31.

For the reasons discussed in § II.D.3 and immediately above, Petitioner demonstrates by a preponderance of evidence how all the limitations of claim 1 are taught by the combined teachings of OneChip and ORT8850 and articulates persuasive reasoning for combining the teachings of these references. Accordingly, Petitioner demonstrates by a preponderance of evidence that claim 1 is unpatentable as obvious over OneChip and ORT8850.

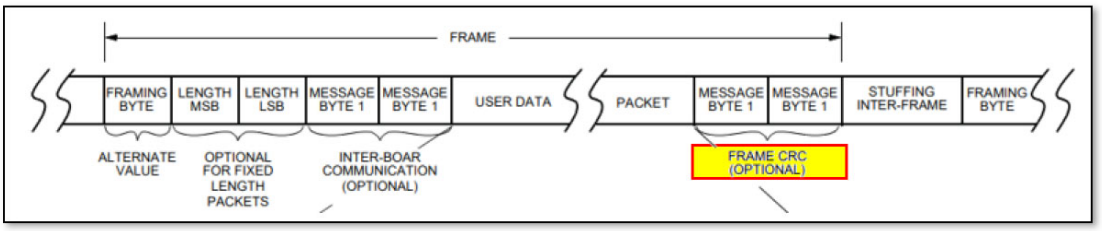
5. Claims 2 and 3

Claim 2 depends from claim 1 and requires "one of said components" of each of the transceivers of claim 1 to be a CRC generator. Ex. 1001, 6:52–53. Claim 3 depends from claim 1 and requires "one of said components" of each of the transceivers of claim 1 to be a CRC verification block. As discussed in § II.C.2, *supra*, because we construe each of the "one of said components" of the transceiver recited in claim 1 to have selectable values and to be configured by memory, the CRC generator and verification blocks required by claims 2 and 3, respectively, must also have selectable values and be configured by memory.

Notwithstanding Patent Owner's arguments to the contrary, discussed *infra*, Petitioner demonstrates how ORT8850 teaches the limitations required by claims 2 and 3. *See* Pet. 45–47; Pet. Reply 9–11. Petitioner argues "ORT8850 explains that its device 'facilitates high-speed serial transfer of data in a variety of applications including Gigabit Ethernet, fibre channel, serial backplanes, and proprietary links.'" Pet. 46 (quoting Ex. 1005, 17) (emphases omitted). Relying on the testimony of Dr. Nelson, Petitioner argues a person skilled in the art would have "appreciate[d] that CRC

generation is a feature of supporting at least Gigabit Ethernet and Fibre Channel because each protocol requires transmitted packets to include CRC values." *Id.* (citing Ex. 1003 ¶ 75). Petitioner argues that an ORT8850 Application Note confirms that contention by "showing ORT8850's framers—which are 'designed to be easily connected to any user specific application'—include an optional 'Frame CRC.'" *Id.* (emphasis omitted) (quoting Ex. 1015, 6). For the same reason—i.e., support of both Gigabit Ethernet and Fibre Channel protocols—Petitioner argues a person skilled in the art would have known that ORT8850 also includes a "CRC checking or verification" block. *Id.* at 47 (citing Ex. 1003 ¶¶ 80–81).

We agree with Petitioner. ORT8850 expressly discloses that it supports the Gigabit Ethernet and Fibre Channel protocols. Ex. 1005, 17. Moreover, we agree with Dr. Nelson that a person skilled in the art would have understood that "CRC generation" and "CRC checking" are "feature[s] of supporting at least Gigabit Ethernet and Fibre Channel because each protocol requires transmitted packets to include CRC values." Ex. 1003 ¶¶ 75, 80. Indeed, one way the '709 patent discloses configuring CRC generator 152 and CRC verification block 186 is by selecting either Gigabit Ethernet or Fibre Channel protocol. Ex. 1001, 3:43–51, 5:51–58. A second way the '709 patent discloses configuring these blocks is by using or bypassing them. *Id.* The ORT8850 transceivers similarly disclose that their CRC generator and verification blocks can be used or bypassed, as illustrated in Figure 6 of an ORT8850 Application Note, a Petitioner-colorized version of which is reproduced below. *See* Pet. Reply 10; Ex. 1015, 1, 6.



The figure above is a Petitioner-colorized version of Figure 6 of an ORT8850 Application Note. Ex. 1015, 6, Fig. 6. As shown in the figure, a frame that is transmitted/received by an ORT8850 transceiver can contain *optional* CRC verification information. *Id.*, Fig. 6. Thus, ORT8850's CRC generator and verification blocks can be optionally used or bypassed depending on whether optional CRC information is included in a transmitted frame or available to be checked in a received frame.

Patent Owner argues Petitioner has failed to demonstrate the unpatentability of claims 2 and 3 for the reasons discussed above with respect to claim 1. *See* PO Resp. 11. We disagree for the reasons stated in § II.D.3–4, *supra.* Patent Owner further argues that Petitioner has failed to demonstrate the unpatentability of claims 2 and 3 because "Petitioner and Dr. Nelson merely assert that ORT8850's transceivers would include the recited components—not that the components would 'hav[e] selectable values.'" *Id.* at 11–12. We disagree for the reasons stated above. Petitioner has shown ORT8850 includes CRC generator and verification blocks that are configurable and have selectable values because they can (a) be bypassed or (b) include the CRC information required by either the Gigabit Ethernet or Fibre Channel protocols. *See* Pet. 45–47; Pet. Reply 9–11.

For the reasons discussed in § II.D.3 and immediately above, Petitioner demonstrates by a preponderance of evidence how all the limitations of claims 2 and 3 are taught by the combined teachings of

OneChip and ORT8850 and articulates persuasive reasoning for combining the teachings of these references. Accordingly, Petitioner demonstrates by a preponderance of evidence that claims 2 and 3 are unpatentable as obvious over OneChip and ORT8850.

6. Claims 4 and 5

Claim 4 requires the deserializer of claim 1 to include a configurable comma detection function. Ex. 1001, 6:56–58. Claim 5 requires "one of said components" of claim 1 to be an elastic buffer. *Id.* at 6:59–60. Petitioner demonstrates how ORT8850 teaches the limitations required by claims 4 and 5. *See* Pet. 47–49 (citing Ex. 1005, 12, 17, Fig. 3; Ex. 1003 ¶¶ 82–87).

ORT8850 discloses that when it decodes 8B/10B encoded data its deserializer "align[s] multiple channels on the K28.5 (comma) character boundary." Ex. 1005, 17. The function that detects this K28.5 character boundary is configurable via the COMMADET and ENCOMMA signals. *See* Ex. 1005, 19, Fig. 3. We agree with Dr. Nelson that the ENCOMMA signal is the signal stored in the CRD specific register having hexadecimal address e3, which enables/disables the comma detection function. *See* Ex. 1003 ¶ 83 (citing Ex. 1005, 45). ORT8850 further discloses that its transceivers use "[e]lastic buffers . . . to align each incoming STS-12 link." Ex. 1005, 12. Patent Owner does not dispute Petitioner's specific contentions regarding claims 4 and 5 but instead argues these claims are patentable for the reasons discussed above with respect to claim 1. *See* PO Resp. 8–32; PO Sur-Reply 3–22. We disagree for the reasons discussed in § II.D.3–4*, supra.*

For the reasons discussed in § II.D.3 and immediately above, Petitioner demonstrates by a preponderance of evidence how all the

limitations of claims 4 and 5 are taught by the combined teachings of OneChip and ORT8850 and articulates persuasive reasoning for combining the teachings of these references. Accordingly, Petitioner demonstrates by a preponderance of evidence that claims 4 and 5 are unpatentable as obvious over OneChip and ORT8850.

7. Claims 8–12

Claim 8 recites an integrated circuit that is substantially similar to the integrated circuit recited in claim 1. *Compare* Ex. 1001, 6:25–51, *with id. at* 7:1–19. Both claims require configurable transceivers having configurable serializers/deserializers to transmit/receive data at a selected rate and input/output ports that receive/transmit differential input/output signals. *Compare id.* at 6:38–46, *with id.* at 7:8–15. Both claims require the transceivers to include a LOS detector; however, claim 8 does not require the LOS detector to have selectable values and be configurable via memory. *Compare id.* at 6:32–36, *with id.* at 7:4–7. Both claims require a programmable fabric; however, claim 8 includes a processor core and requires the programmable fabric to surround the processor core rather than to couple to configuration memory. *Compare id.* at 6:25–30, *with id.* at 7:1–3. Finally, both claims require a plurality of signal paths passing through the programmable fabric; however, claim 8 requires the signal paths to couple at least one transceiver to the processor core rather than to a circuit that has been implemented in the programmable fabric. *Compare id.* at 6:47–51, *with id.* at 7:16–19.

Given the substantial similarity between claims 1 and 8, Petitioner demonstrates how the claim 8 limitations that are common to claim 1 are met via its analysis of claim 1. *See* Pet. 49–55; *see also* § II.D.4, *supra*. Petitioner also demonstrates how the combination of OneChip and ORT8850

teaches the claim 8 limitations that are not recited in claim 1, including a processor core surrounded by a programmable fabric having transceivers located at its periphery and signal paths passing through the programmable fabric to connect at least one transceiver to the processor core. *See* Pet. 49–55 (citing Ex. 1004, 126, 130–132, Fig. 6; Ex. 1005, Fig. 1).

Specifically, Petitioner demonstrates how OneChip teaches the claim 8 limitations not recited in claim 1 with a colorized version of OneChip's Figure 6, which is reproduced below. *Id.* at 54.

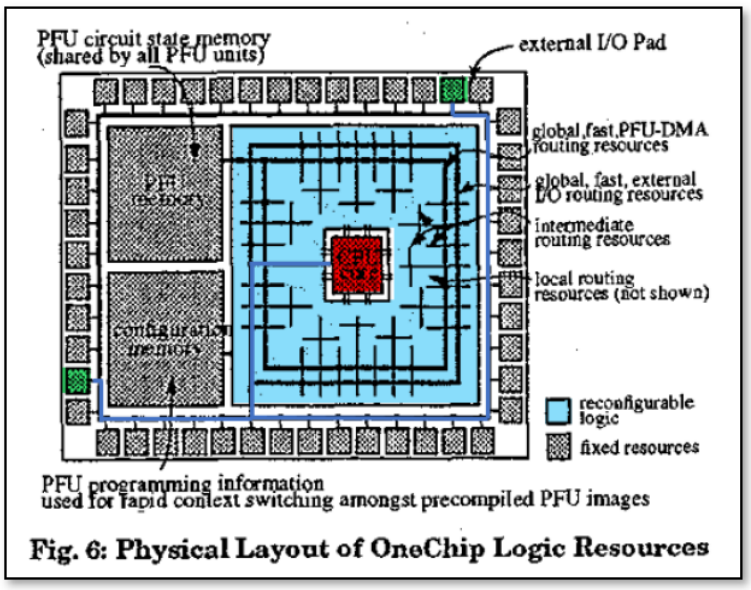


Fig. 6: Physical Layout of OneChip Logic Resources

The figure above is a Petitioner-colorized version of Figure 6 of OneChip. It illustrates how OneChip discloses a processor core (red) surrounded by a programmable fabric (light blue) having peripheral I/O pads (green) and a plurality of signal paths (dark blue) through the programmable fabric (light blue) that connect I/O pads (green) to the processor core (red). *Id.* As discussed in § II.D.3, *supra*, Petitioner proposes modifying OneChip to include ORT8850's peripherally located configurable transceivers so that the result would "hav[e] a processor core surrounded by a programmable fabric

with I/O circuits at the periphery, with I/O signals connected to the processor core through the fabric." Pet. 23.

Claim 9 depends from claim 8 and adds to claim 8 limitations that are substantially similar to limitations recited in claim 1 (i.e., configuration memory cells, some of which are associated with the configurable transceivers). *Compare* Ex. 1001, 7:20–23, *with id.* at 6:26, 6:32–35. Claim 10 depends from claim 9 and adds to claim 9 the same limitation that claims 2 and 3 add to claim 1 (i.e., transceiver CRC generator and verification blocks). *Compare id.* at 7:24–27, *with id.* at 6:52–55. Claim 11 depends from claim 8 and adds to claim 8 the same limitation that claim 4 adds to claim 1 (i.e., the deserializer includes a configurable comma detection function). *Compare* Ex. 1001, 7:28–30, *with id.* at 6:56–58. Claim 12 depends from claim 9 and adds to claim 9 the same limitation that claim 5 adds to claim 1 (a configurable transceiver includes an elastic buffer). *Compare* Ex. 1001, 7:31–33, *with id.* at 6:59–60. Given the substantial similarity between claim 9 and claim 1, claim 10 and claims 2 and 3, claim 11 and claim 4, and claim 12 and claim 5, Petitioner demonstrates how the limitations required by claims 9–12 are met via its analyses of claims 1–5. *See* Pet. 55–56; *see also* §§ II.D.4–6, *supra*.

Patent Owner argues claims 8–12 are patentable over OneChip and ORT8850 for the reasons discussed in § II.D.3, *supra*, i.e., because OneChip is not enabled and a person of ordinary skilled in the art would not have (a) replaced OneChip's allegedly parallel-only I/O circuitry with ORT8850's SERDES, (b) coupled OneChip's FPGA memory to ORT8850's non-FPGA SERDES, and (c) combined OneChip and ORT8850 with reasonable expectation of success. *See* PO Resp. 12–27; PO Sur-Reply 16–19. We disagree for the reasons discussed in § II.D.3.

For the reasons discussed in § II.D.3 and immediately above, Petitioner demonstrates by a preponderance of evidence how all the limitations of claims 8–12 are taught by the combined teachings of OneChip and ORT8850 and articulates persuasive reasoning for combining the teachings of these references. Accordingly, Petitioner demonstrates by a preponderance of evidence that claims 8–12 are unpatentable as obvious over OneChip and ORT8850.

8. Claims 15–17

Claim 15 recites an IC that is substantially similar to the ICs recited in claims 1 and 8. *Compare* Ex. 1001, 8:4–26, *with id.* at 6:25–51 and 7:1–19. Like claim 8, claim 15 requires a processor core and a programmable fabric, but claim 15 does not require the programmable fabric to surround the processor core. *Compare id.* at 8:10–12, *with id.* at 7:2–3. Like claim 1, claim 15 requires a plurality of configuration memory cells to implement a circuit in the programmable fabric. *Compare id.* at 8:5–8, *with id.* at 6:26–31. Like claim 8, claim 15 requires configurable transceivers located at the periphery of the programmable fabric and having configurable serializers/deserializers to transmit/receive data at a selected rate; however, claim 15 does not require the transceivers to have input/output ports that receive/transmit differential input/output signals and does not require at least one transceiver to have a LOS detector. *Compare id.* at 8:14–21, *with id.* at 7:4–15. Finally, like claim 8, claim 15 requires a plurality of signal paths passing through the programmable fabric, at least one of which couples a transceiver to the processor core. *Compare id.* at 8:23–26, *with id.* at 7:16–19. Given the substantial similarity between claim 15 and claims 1 and 8, Petitioner demonstrates how the limitations required by claim 15 are met via

its analyses of claims 1 and 5. *See* Pet. 56–59; *see also* §§ II.D.4 and II.D.7, *supra*.

Claim 16 depends from claim 15 and adds to claim 15 a limitation that is substantially similar to the limitation claim 4 adds to claim 1 (i.e., each deserializer has a configurable comma detection function). *Compare* Ex. 1001, 8:27–30, *with id.* at 6:55–57. Claim 16 differs from claim 4 by requiring the comma detection function to detect one of at least two different definitions of a comma. *Id. at* 8:27–30. Petitioner demonstrates how ORT8850 teaches this limitation. *See* Pet. 47–48, 59–60, 80. Specifically, Petitioner demonstrates that "ORT8850 discloses that its 'HSI will detect and align to either polari[t]y of the K28.5' (i.e., the comma character)." *Id.* at 59–60 (quoting Ex. 1005, 17) (emphasis omitted). Patent Owner does not dispute this contention. *See* PO Resp. 12–32; PO Sur-Reply 16–22.

Claim 17 depends from claim 15 and adds to claim 15 a limitation that is recited in claims 1 and 8 (i.e., at least one transceiver includes a LOS detector). *Compare* Ex. 1001, 8:31–33, *with id.* at 7:5–7. Given this substantial similarity, Petitioner demonstrates how the limitation required by claim 17 is met via its analysis of claim 1. *See* Pet. 60; *see also* § II.D.4, *supra*.

Patent Owner argues claims 15–17 are patentable over OneChip and ORT8850 for the reasons discussed in § II.D.3, *supra*. *See* PO Resp. 12–27; PO Sur-Reply 16–19. We disagree for the reasons discussed there.

For the reasons discussed in § II.D.3 and immediately above, Petitioner demonstrates by a preponderance of evidence how all the limitations of claims 15–17 are taught by the combined teachings of OneChip and ORT8850 and articulates persuasive reasoning for combining the teachings of these references. Accordingly, Petitioner demonstrates by a

preponderance of evidence that claims 15–17 are unpatentable as obvious over OneChip and ORT8850.

E. Challenges Based on Chan, ORT8850, and OneChip

Petitioner argues claims 1–5, 8–12, and 15–17 are unpatentable as obvious over Chan, OneChip and ORT8850. Pet. 60–80; Pet. Reply 23–28. Patent Owner disagrees. PO Resp. 32–48; PO Sur-Reply 22–25. For the reasons discussed in § II.D, *supra*, Petitioner has shown by a preponderance of evidence that these claims are unpatentable over OneChip and ORT8850. This finding is dispositive of Petitioner's challenge to the patentability of claims 1–5, 8–12, and 15–17. Accordingly, we need not address whether Petitioner has further shown, by a preponderance of evidence, that these claims are also unpatentable as obvious over the combination of Chan, OneChip, and ORT8850. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue).

F. Challenges Based on OneChip, ORT8850, and QL80FC and Based on Chan, ORT8850, OneChip and QL80FC

Petitioner argues claims 1–3, 6–8, 10, 13, 14, and 17 are unpatentable as obvious over OneChip, ORT8850, and QL80FC, with or without Chan. Pet. 80–94; Pet. Reply 20–23, 28–30. Patent Owner disagrees. PO Resp. 48–58; PO Sur-Reply 25–27. For the reasons discussed in § II.D, *supra*, Petitioner has shown by a preponderance of evidence that claims 1–3, 8, 10–12, and 17 are unpatentable over OneChip and ORT8850. This finding is dispositive of Petitioner's challenge to the patentability of these claims. Accordingly, we need not address whether Petitioner has also shown that these claims also unpatentable over the combination of OneChip, ORT8850, and QL80FC, with or without Chan. *See Beloit*, 742 F.2d at 1423.

Claim 6 depends from claim 1 and further requires a programmable fabric to generate at least one signal to control the values of the transceiver components required by claim 1. Ex. 1001, 6:61–64. Claim 7 depends from claim 6 and further requires one of the transceiver components to be an encoder controlled by the signal required by claim 6. *Id.* at 6:65–67. Claim 13 depends from claim 8 and further requires the programmable fabric to generate a signal to control at least one configurable transceiver required by claim 8. *Id.* at 7:34–36. Claim 14 depends from claim 13 and further requires the configurable transceiver to include an encoder controlled by the signal required by claim 13. *Id.* at *8*:1–3.

Petitioner relies solely on QL80FC to teach the limitations required by claims 6, 7, 13, and 14. *See* Pet. 90–94 (citing Ex. 1008, 1, 8, Figs. 1–4). For the reasons discussed in § II.A.3, *supra,* we exclude QL80FC because Petitioner has failed to demonstrate its authenticity.[13] For this reason, Petitioner has failed to demonstrate by a preponderance of evidence that claims 6, 7, 13, and 14 are unpatentable over OneChip, ORT8850, and QL80FC, with or without Chan.

III. CONCLUSION

We have reviewed the Petition, Patent Owner Response, Petitioner Reply, and Patent Owner Sur-Reply. We have considered all the evidence and arguments presented by Petitioner and Patent Owner. We find, on this

[13] Petitioner argues we should not exclude Exhibit 1008 because "Dr. Nelson review and relied upon this exhibit in reaching his opinions." Opp. 14. To the contrary, Dr. Nelson's opinion is that QL80FC discloses the limitations of claims 6, 7, 13, and 14. *See* Ex. 1003 ¶ 192 (claim 6, "QL80FC discloses this limitation."), ¶ 193 (claim 7, same), ¶ 196 (claim 13, "QL80FC discloses this claim"), ¶ 197 ("QL80FC discloses a loss of synchronization detector in further detail.").

record, Petitioner has demonstrated by a preponderance of evidence that claims 1–5, 8–12, 15–17 of the '709 patent are unpatentable over OneChip and ORT8850 but has failed to demonstrate by a preponderance of evidence that claims 6, 7, 13, and 14 of the '709 patent are unpatentable over OneChip, ORT8850, and QL80FC, with or without Chan.

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–5, 8–12, 15–17	103(a)	OneChip, ORT8850	1–5, 8–12, 15–17	
1–5, 8–12, 15–17	103(a)	Chan, ORT8850, OneChip[14]		
1–3, 6–8, 10, 13, 14, 17	103(a)	OneChip, ORT8850, QL80FC[15]		6, 7, 13, 14
1–3, 6–8, 10, 13, 14, 17	103(a)	Chan, ORT8850, QL80FC, OneChip[16]		6, 7, 13, 14
Overall Outcome			1–5, 8–12, 15–17[17]	6, 7, 13, 14

[14] Because Petitioner has demonstrated the unpatentability of these claims over OneChip and ORT8850, we do not determine their patentability over Chan, OneChip, and ORT8850.
[15] Because Petitioner has demonstrated that claims 1–3, 8, 10, and 17 are unpatentable over OneChip and ORT8850, we do not determine the patentability of these claims over OneChip, ORT8850, and QL80FC.
[16] Because Petitioner has demonstrated that claims 1–3, 8, 10, and 17 are unpatentable over OneChip and ORT8850, we do not determine the patentability of these claims over Chan, OneChip, ORT8850, and QL80FC.
[17] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has demonstrated by a preponderance of evidence that claims 1–5, 8–12, 15–17 of the '709 patent are unpatentable;

FURTHER ORDERED that Petitioner has failed to show, on this record, that claims 6, 7, 13, and 14 of the '709 patent are unpatentable over OneChip, ORT8850, and QL80FC, with or without Chan;

FURTHER ORDERED that Patent Owner's motion to exclude Exhibit 1005 for hearsay or lack of authentication is denied;

FURTHER ORDERED that Patent Owner's motion to exclude paragraphs 4, 5, 10–15, and 17–20 and Exhibits A–F and J of Exhibit 1018 for hearsay and lack of authentication is denied;

FURTHER ORDERED that Patent Owner's motion to exclude paragraph 22 and Exhibits G–I of Exhibit 1018 is dismissed as moot;

FURTHER ORDERED that Patent Owner's motion to exclude Exhibit 1008 is granted;

FURTHER ORDERED that Patent Owner's motion to exclude Exhibits 1012 and 1033 is dismissed as moot; and

FURTHER ORDERED that this Decision is final, and a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

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